



Department of Signal Processing



Jiří Kadlec

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kadlec@utia.cas.cz

Evaluation of the team 2015-19

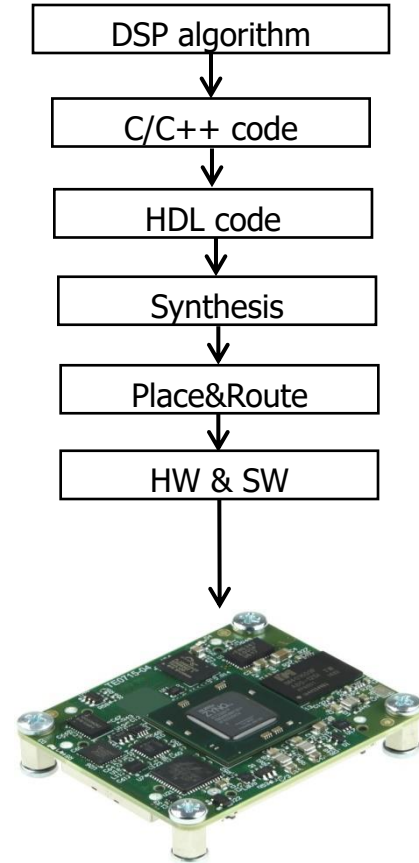
Overview of the Department

▷ Topics

- ▷ Recursive system identification in digital signal processing (DSP)
- ▷ Systolic arrays, dedicated arithmetic, SW & HW
- ▷ Field programmable gate arrays (FPGA)
- ▷ Dynamically reprogrammable FPGA accelerators
- ▷ Embedded systems,
- ▷ Human-machine-interfaces (HMI)

▷ Strengths

- ▷ Algorithmic engineering for DSP applications
- ▷ HW design of intellectual property (IP) for FPGA
- ▷ Strong track record of research cooperation in EU R&D projects.
- ▷ Contract-based industrial research.
- ▷ Mainly in HMI in cooperation with Skoda Auto.



Overview of the Department

▷ Department staff

- ▷ Ing. Jiří Kadlec, CSc. (1.0) Head of Department, DSP
- ▷ Ing. Zdeněk Pohl, Ph.D. (1.0) Deputy head of Department, DSP
- ▷ Ing. Lukáš Kohout (1.0) FPGA design
- ▷ Ing. Radim Matulík (1.0) HW, PCB design
- ▷ Doc. Ing. I. Nagy, CSc. (0.64) Bayesian mixtures, teaching CTU
- ▷ Doc. Ing. E. Uglickich, CSc. (1.0) Bayesian mixtures, teaching CTU
- ▷ Ing. Raissa Likhonina (1.0) Ph.D. student
- ▷ Dr. Ing. Jiří Plíhal (1.0) Deputy head of Department for Internal projects with Škoda Auto
- ▷ Ing. David Pavlík Ph.D. (1.0) Internal projects with Škoda Auto
- ▷ Ing. Gabriela Havlíčková (1.0) Internal projects with Škoda Auto
- ▷ Bc. Veronika Kyznarová (1.0) Internal projects with Škoda Auto
- ▷ Mgr. Milada Kadlecová (1.0) Secretary
- Total (11.64)

Overview of the Department

Publications 2015-2019

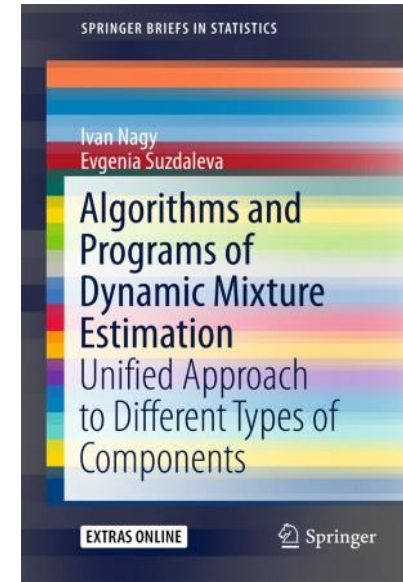
Books	Chapters in books	Journal articles	Conference Papers	App Notes, Eval. Packages
1	5	10	21	60

Book

- ▷ [Nagy Ivan, Suzdaleva Evgenia : Algorithms and Programs of Dynamic Mixture Estimation. Unified Approach to Different Types of Components](#), Springer, (Cham 2017) SpringerBriefs in Statistics [2017] DOI: [10.1007/978-3-319-64671-8](#) (Note: Evgenia Suzdalova changed her name to Evženie Uglickich)

Three selected journal articles

- ▷ [Suzdaleva Evženie, Nagy Ivan : Two-layer pointer model of driving style depending on the driving environment](#) , *Transportation Research. Part B: Methodological* vol.128, 1 (2019), p. 254-270 [2019] DOI: [10.1016/j.trb.2019.08.009](#)
- ▷ [Suzdaleva Evgenia, Nagy Ivan : An online estimation of driving style using data-dependent pointer model](#) , *Transportation Research. Part C: Emerging Technologies* vol.86, 1 (2018), p. 23-36 [2018] DOI: [10.1016/j.trc.2017.11.001](#)
- ▷ [Hoozemans J., Van Straten J., Viitanen T., Tervo A., Kadlec Jiří, Al-Ars Z. : ALMARVI Execution Platform: Heterogeneous Video Processing SoC Platform on FPGA](#) , *Journal of Signal Processing Systems for Signal Image and Video Technology* vol.91, 1 (2019), p. 61-73 [2019] DOI: [10.1007/s11265-018-1424-1](#)



Overview of the Department

Evaluation Packages & Application Notes <http://zs.utia.cas.cz/>

- ▶ Department overview
- ▶ Details about projects
- ▶ Evaluation package download server
- ▶ Application note download
- ▶ Licensing conditions

The screenshot shows the homepage of the FITOptiVis department. The header includes the logo and the slogan "Creativity with Ideas". A navigation menu on the left lists various sections: News, Profile, Presentations, EU R&D Projects, National R&D Projects, Industrial research, Support Projects, Downloads, Staff, Contact, and Useful Links. The main content area features the FITOptiVis logo and a title: "From the cloud to the edge - smart Integration and Optimization Technologies for highly efficient Image and Video processing Systems". Below this, there is a detailed description of the project's objectives and goals, followed by a "Project results" section listing several key achievements and publications.

This screenshot displays a specific application note page. The title is "Design Time and Run Time Resources for Zynq Ultrascale+ TE0808-04-15EG-1EE with SDSoc 2018.2 Support". The page is structured with sections for "Description", "Package Summary", "Revision history", and "Contact Person". The "Description" section provides technical details about the Zynq Ultrascale+ board and the specific design. The "Package Summary" section includes a table with columns for Title, Filename, License, Package content, Size, Required tools & platform, and Installation. The "Revision history" section contains a table with columns for Rev., Date, Author, and Description. At the bottom, there is a "Contact Person" section with contact information for Jiri Kadlec.

This screenshot shows the "Application Note" page, which is a simplified version of the previous page. It prominently displays the title "Design Time and Run Time Resources for Zynq Ultrascale+ TE0808-04-15EG-1EE with SDSoc 2018.2 Support" and the authors' names: Jiří Kadlec, Zdeněk Pohl, and Lukáš Kohout. Below the title, there is a "Revision history" table with the following data:

Rev.	Date	Author	Description
0	11.04.2019	J. Kadlec	Initial draft
1			
2			

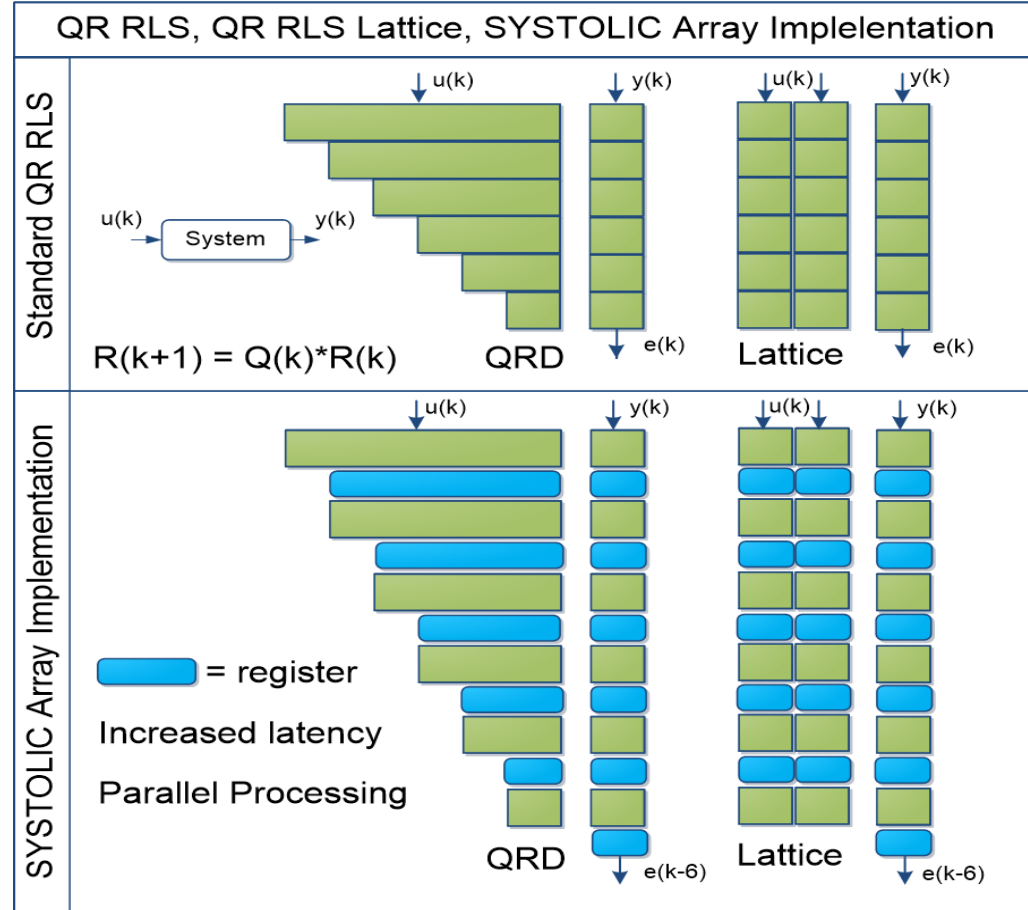
QR RLS Algorithms → Systolic Arrays

▶ Results

- ▶ Matlab C MEX tbx.
- ▶ SciLab C MEX tbx.
- ▶ ARM A9 SciLab C
- ▶ ARM A53 SciLab C
- ▶ STM32H7 QR RLS
STM32Cube tbx.
- ▶ Parallel, C Pthread SW
implementations of
QR RLS Lattice algorithms
on ARM A9 and ARM A53

1 Eval. Package

http://sp.utia.cz/index.php?ids=results&id=dsp_1_6

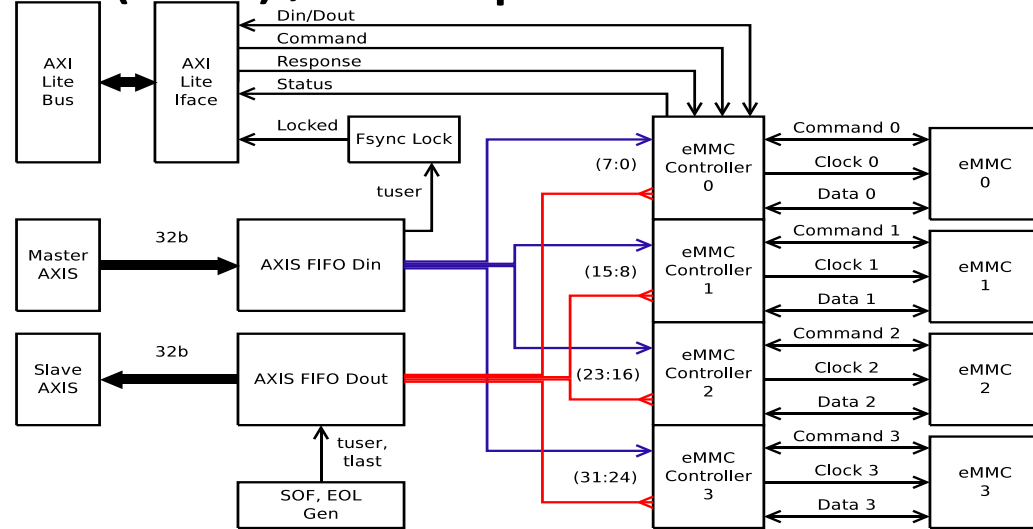


External Funding 2015-2019

		2015	2016	2017	2018	2019
IDEAS	(FP7 ENIAC JU)	■	■	■		
ALMARVI	(FP7 ARTEMIS JU)	■	■	■	■	■
EMC2	(FP7 ARTEMIS JU)	■	■	■	■	■
PANACHE	(FP7 ENIAC JU)	■	■	■	■	■
THINGSTODO	(FP7 ENIAC JU)	■	■	■	■	■
SILENSE	(H2020 ECSEL JU)				■	■
PRODUCTIVE4.0	(H2020 ECSEL JU)				■	■
WAKEMEUP	(H2020 ECSEL JU)					■
FITOPTIVIS	(H2020 ECSEL JU)					■
ARROWHEAD TOOLS	(ECSEL JU)					■
iTEAM	(H2020-MSCA-ITN-2015)		■	■	■	■
External funding ECSEL (Mil Kč)		11,683	11,088	6,435	8,714	11,157
External funding ECSEL 2015-19		49,077 Mil Kč = 1,817 Mil €				

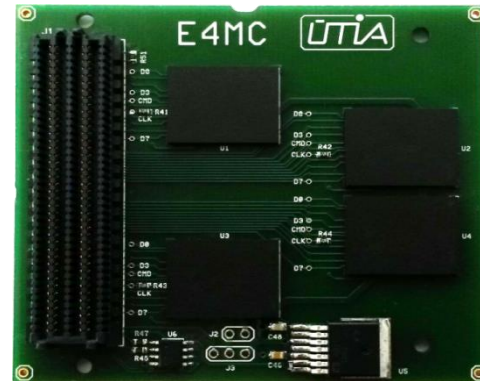
IDEAS – IMA s.r.o. (CZ), 15 partners

- ▶ **Research**
 - ▶ **Micron eMMC Flash devices**
- ▶ **UTIA Results**
 - ▶ **FPGA controller for Micron eMMC Flash devices**
 - ▶ **FMC PCB card**
 - ▶ **SW supporting storage of video from an image sensor in bank of 4 eMMCs.**



2 Eval. Packages

<http://sp.utia.cz/index.php?ids=projects/ideas>



ALMARVI – Philips (NL), 16 partners

▷ Research

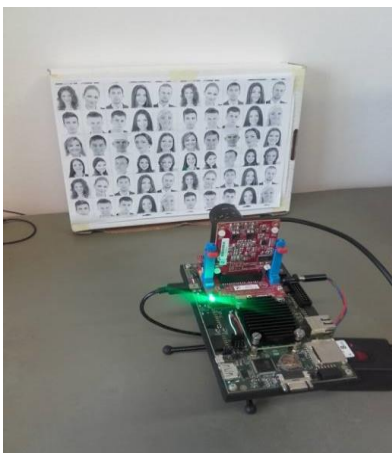
- ▷ HW accele-rated video processing

▷ UTIA Results

- ▷ Support for Xilinx SDSoC
C to HW flow for 28nm Xilinx Zynq industrial modules
- ▷ HW acceleration of the Viola Jones algorithm delivered 5-10 FPS on 28nm Zynq HW

▷ 13 Eval. Packages

<http://sp.utia.cz/index.php?ids=projects/almarvi>



EMC² - Infineon (DE), 100 partners

▷ Research

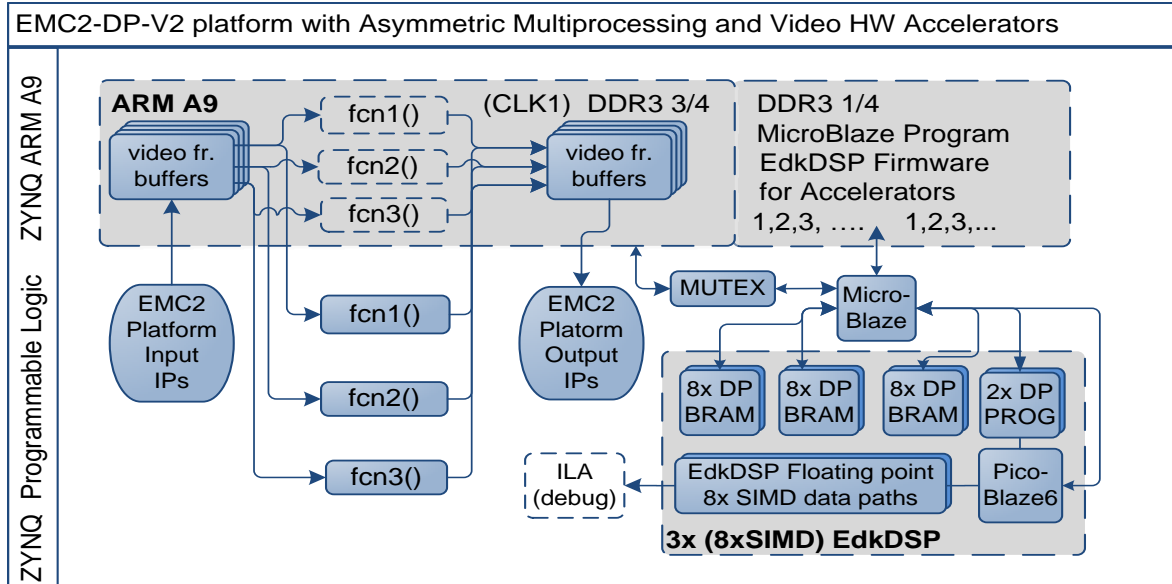
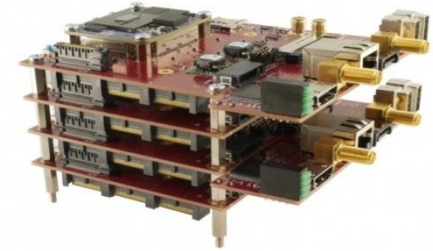
- ▷ MixedCriticality
MultiCore

▷ UTIA Results

- ▷ Support for
Xilinx SDSoC
C to HW flow
EMC2-DP-V2
(Sundance UK)
- ▷ Support for
3x 8xSIMD EdkDSP
FP32 Accelerators

9 Eval. Packages

<http://sp.utia.cz/index.php?ids=projects/emc2>

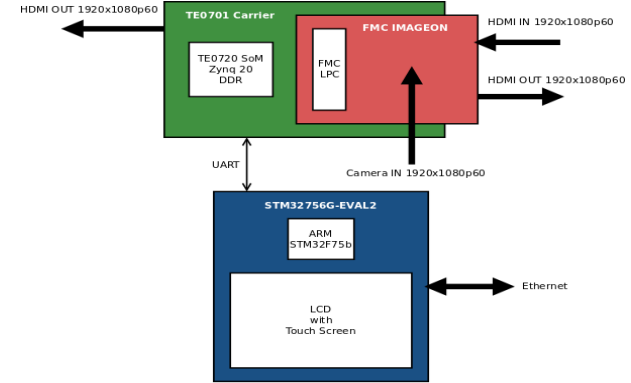


PANACHE – STM (FR), 20 partners

- ▶ **Research**
 - ▶ CMOS 40nm STM32H7 micro-controllers with 2 MBytes on-chip FLASH
- ▶ **UTIA Results**
 - ▶ Terminal with STM32H7 MCU chip and Touch screen GUI
 - ▶ Terminal served for user control of HW-accelerated video processing algorithms running on Xilinx 28 nm Zynq devices.

4 Eval. Packages

<http://sp.utia.cz/index.php?ids=projects/panache>



THINGS2DO – STM (FR), 45 partners

▷ Research

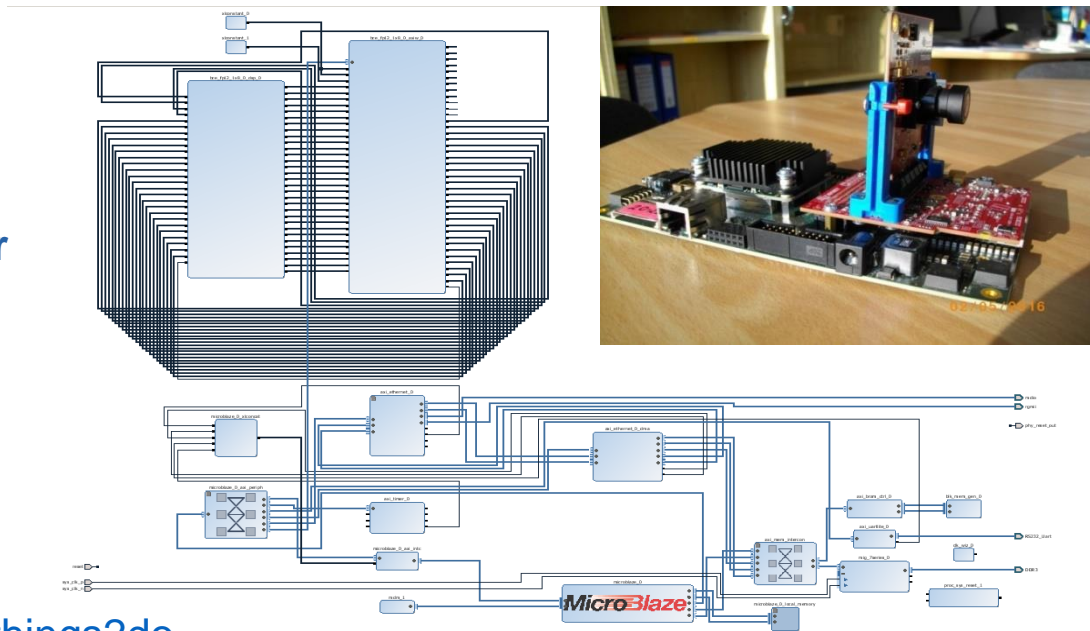
- ▷ Pilot line for the European, low-power 28 nm FD SOI integrated circuits

▷ UTIA Results

- ▷ Model of UTIA 8xSIMD EdkDSP FP HW Accelerator on 28nm Xilinx Artix FPGA
- ▷ It served for the initial power estimation of the EdkDSP IP
- ▷ HW accelerated video processing for the FULL HD video sensor with 60 FPS.

4 Eval. Packages

<http://sp.utia.cz/index.php?ids=projects/things2do>



SILENSE –NXP (BE), 31 partners

▷ Research

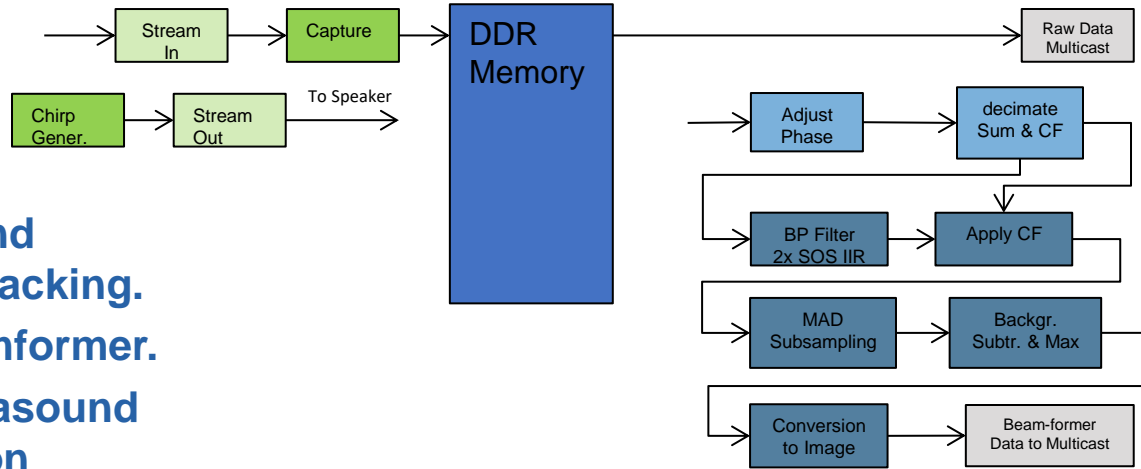
▷ Ultrasound applications

▷ UTIA Results

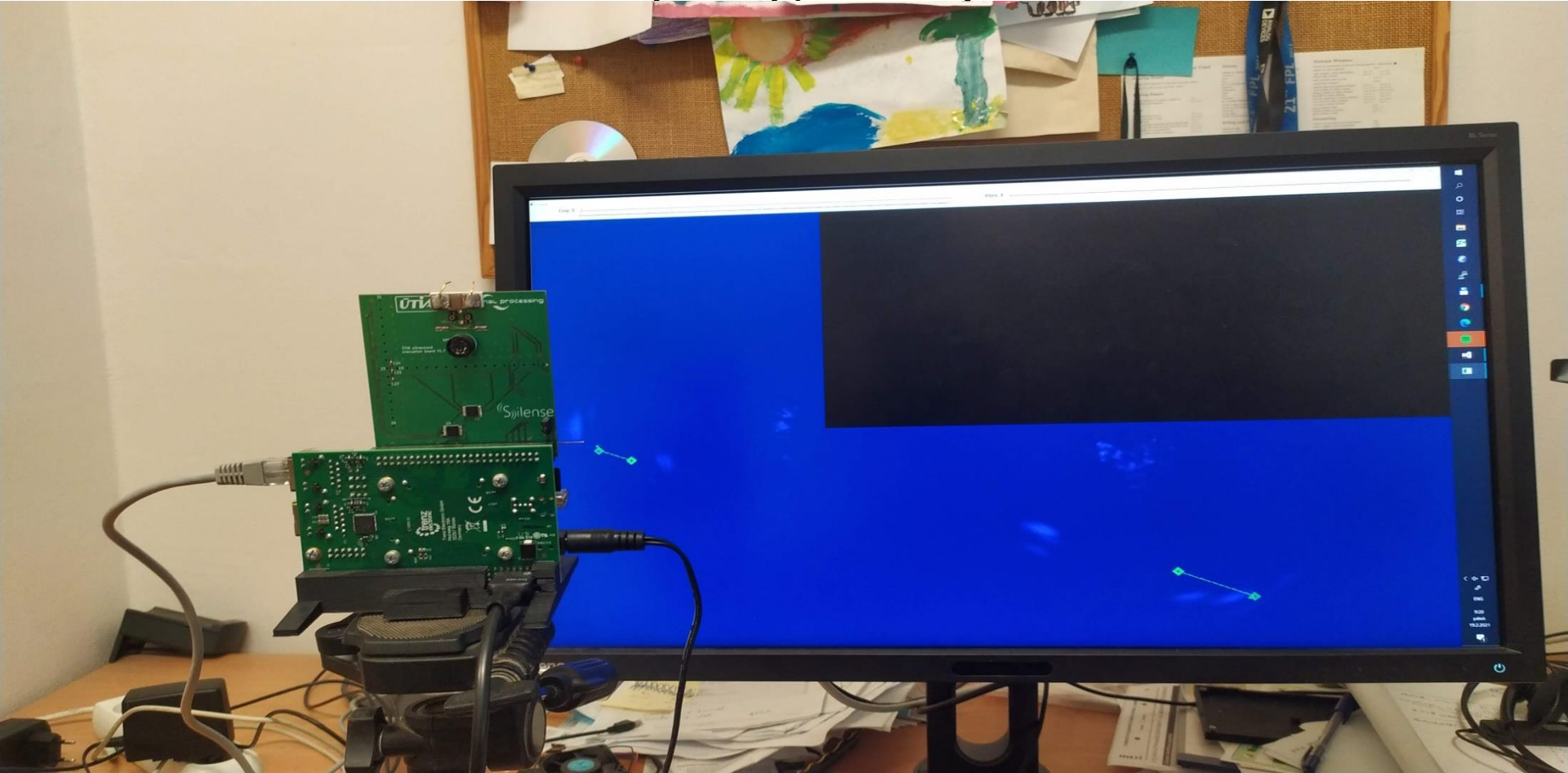
- ▷ HW/SW for an Ultrasound based, Hand-Gesture Tracking.
- ▷ HW 2D ultrasound Beamformer.
- ▷ HW/SW support for ultrasound hand-gesture recognition with the 2D microphone array
- ▷ HW accelerated active noise cancellation.
- ▷ Recursive Hypothesis Testing (in SW).
- ▷ 3 systems have been sold to project partners.

7 Eval. Packages:

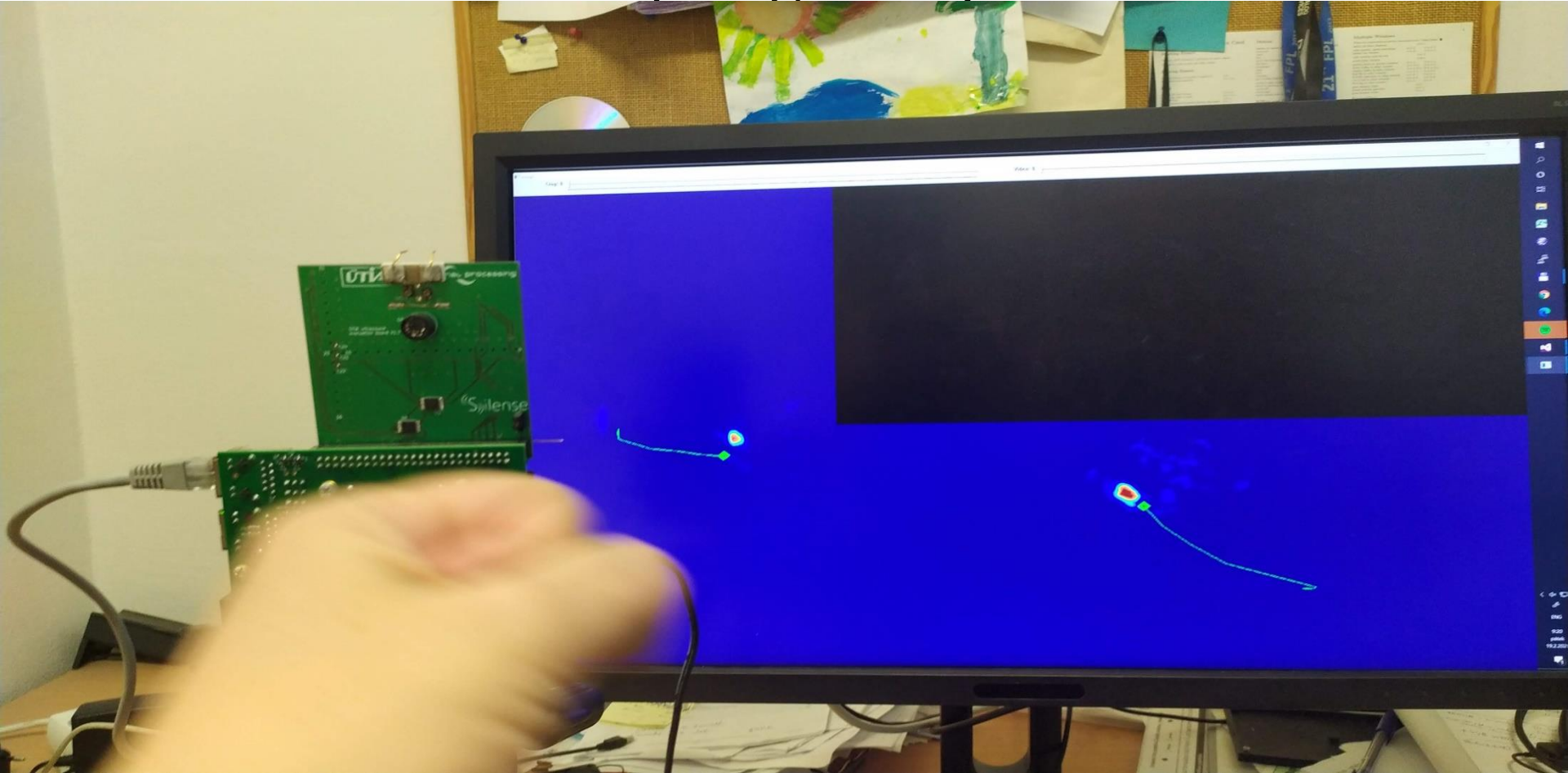
<http://sp.utia.cz/index.php?ids=projects/silense>



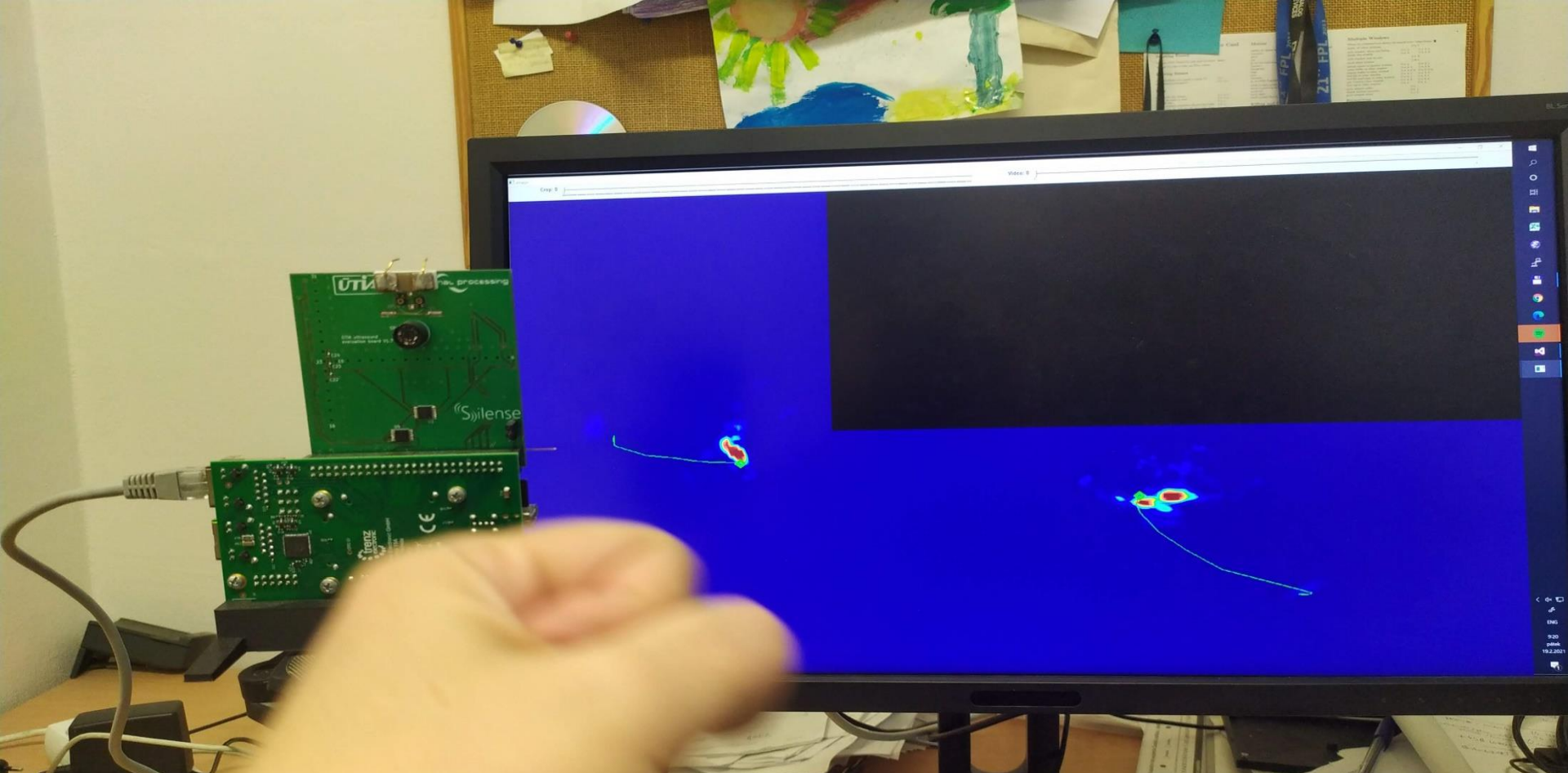
SILENSE –NXP (BE), 31 partners



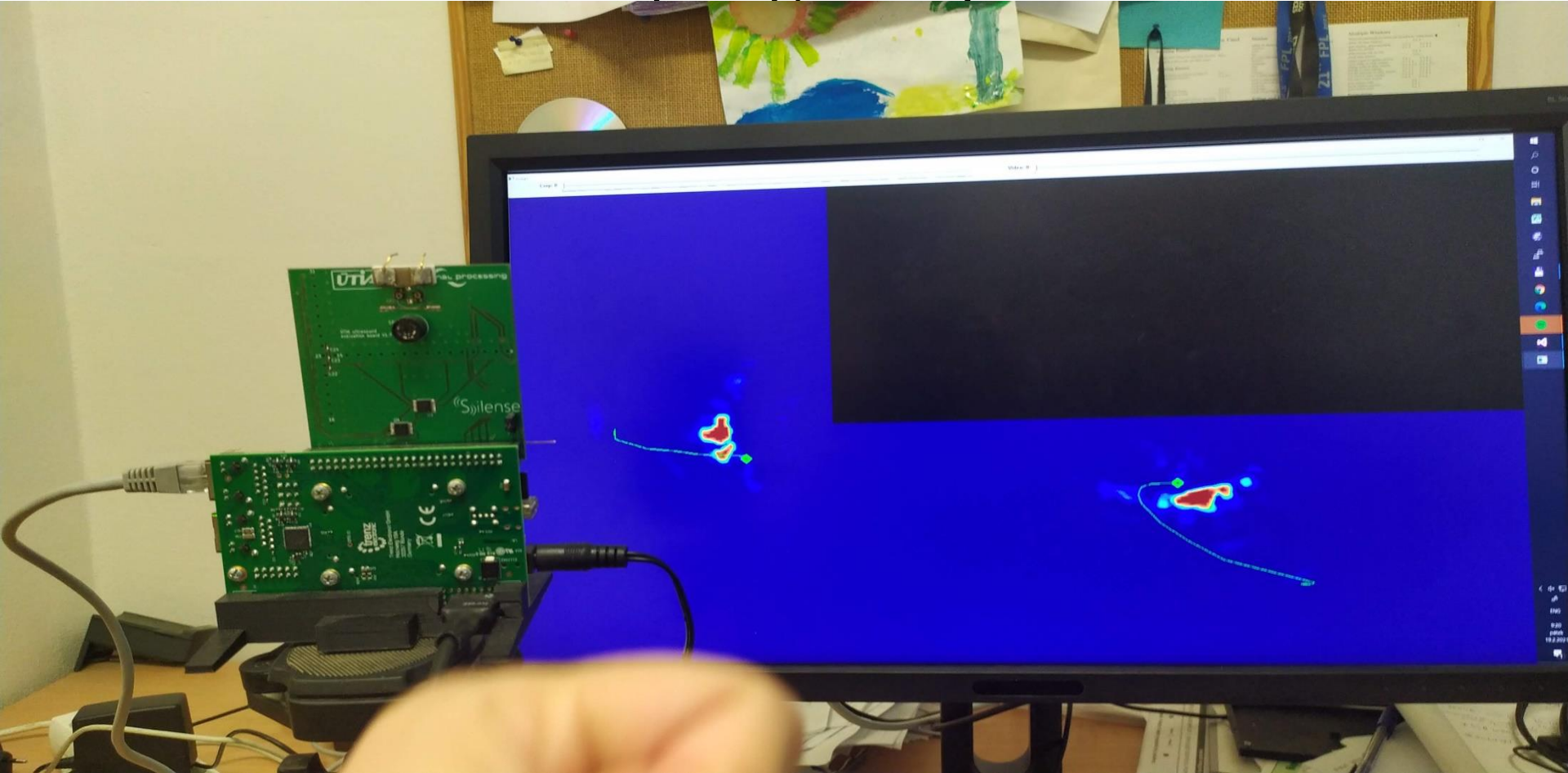
SILENSE –NXP (BE), 31 partners



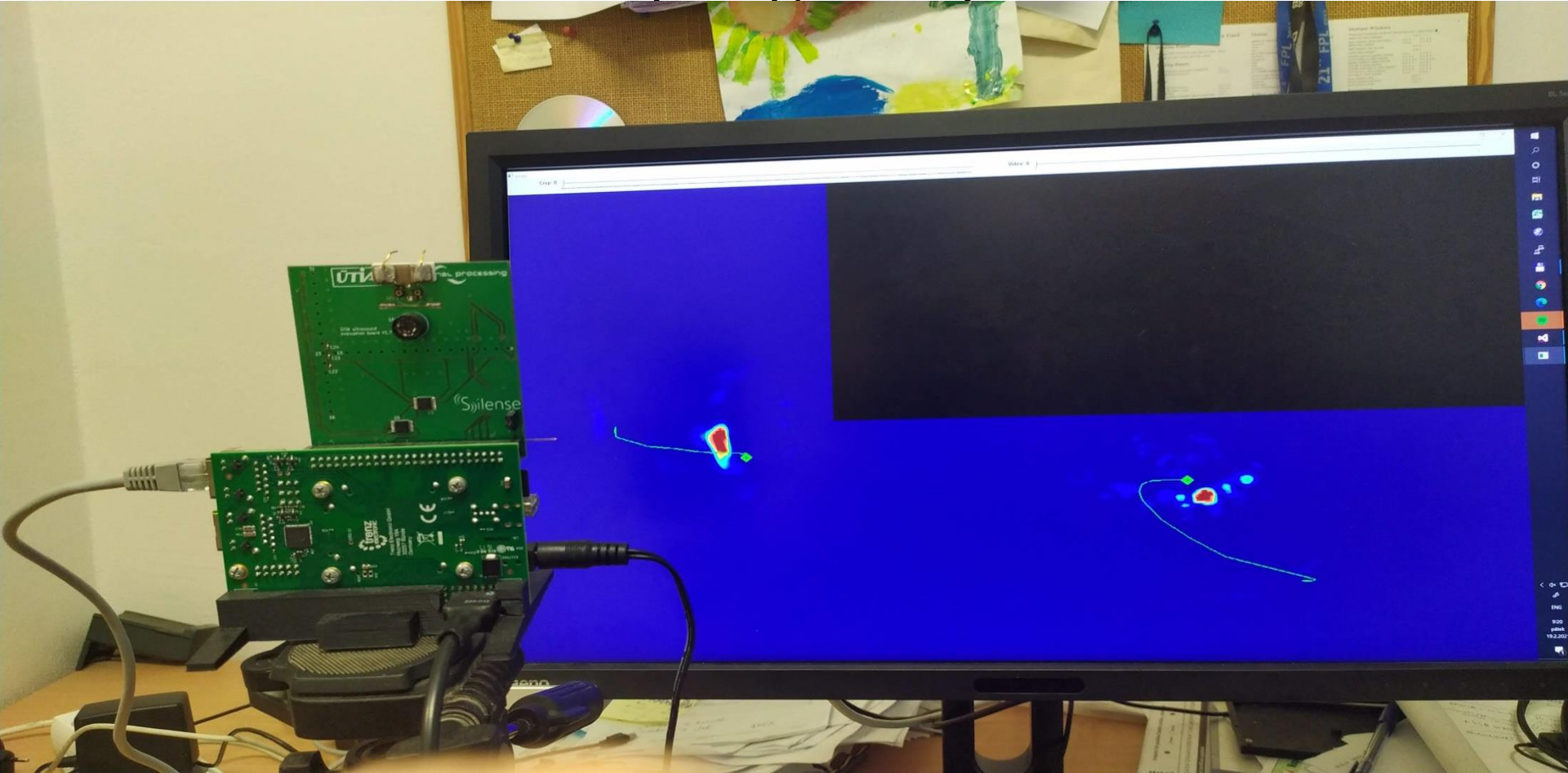
SILENSE –NXP (BE), 31 partners



SILENSE –NXP (BE), 31 partners



SILENSE –NXP (BE), 31 partners



Productive 4.0 – Infineon (DE), 109 p.

▷ Research

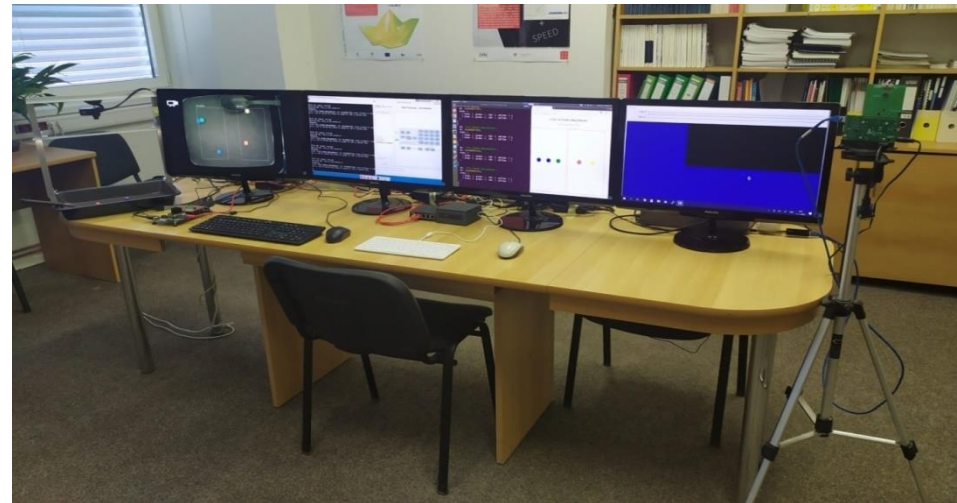
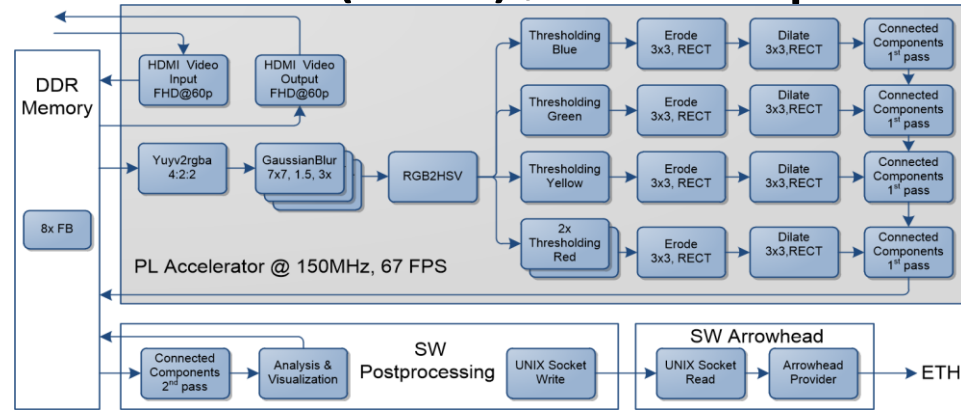
- ▷ Industry 4.0
- ▷ Digitalisation

▷ UTIA Results

- ▷ Ball tracking from the Full HD, 60FPS Video camera data HW accelerated in the 16nm Xilinx Zynq ZU04-EV industrial module.
- ▷ Compatible with ArrowHead 4.0
- ▷ PC: 0.5 FPS
- ▷ Zynq: 60.0 FPS Accelerated 120x

5 Eval. Packages:

<http://sp.utia.cz/index.php?ids=projects/productive40>



Video 1:



WAKeMeUP – STM (FR) ,18 partners

▷ Research

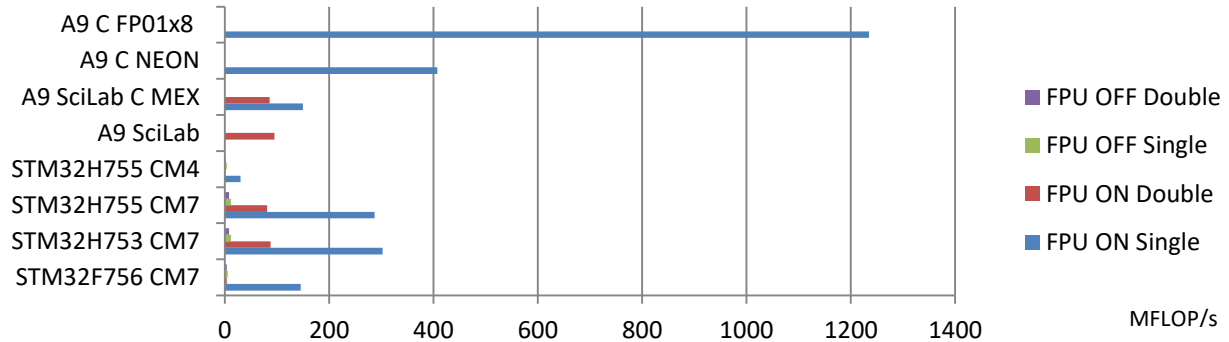
- ▷ STM32H MCU benchmarks

▷ UTIA Results

- ▷ UTIA developed STM32H MCU based terminal with Zynq Debian Linux OS, SciLab and 8xSIMD FP HW accelerator

▷ FP and DP benchmarks:

- ▷ Base: STM32F7 MCUs
- ▷ New: STM32H7 MCUs
- ▷ ARM 2xA9: zcu0710-1c
- ▷ HW encryption bench.
- ▷ DMA benchmarks



4 Eval. Packages:

<http://sp.utia.cz/index.php?ids=projects/wakemeup>

FitOptiVis – Philips (NL), 30 partners

▷ Research

- ▷ From embedded to cloud-based Video Processing

▷ UTIA Results

- ▷ Design time support for 28 nm Xilinx Zynq and 16 nm Zynq Ultrascale+ devices with Xilinx SDSoC C/C++ to HW system-level compiler.
- ▷ Support for UTIA 8x 8xSIMD FP FP32 reconfigurable HW accelerators

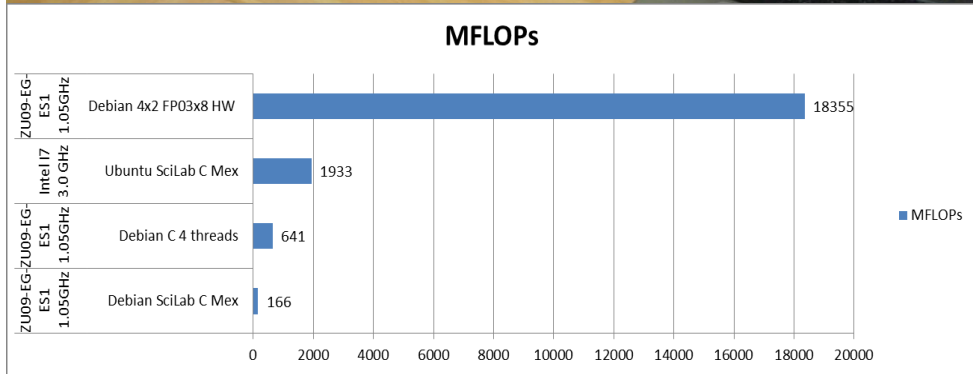
▷ Lucas Kanade Dense Optical Flow, SW/HW:

- ▷ Arm A53, 1.05 GHz SW:
0.1 FPS
- ▷ Zynq zu15-eg-1e 250 MHz HW:
60.0 FPS **600x**
- ▷ In paraleel with HW accelerated
Matrix Multiplication FP32: **110x**

9 Eval. Packages:

Video 2:  video2.MP4

<http://sp.utia.cz/index.php?ids=projects/fitoptivis>



FitOptiVis – Philips (NL), 30 partners

▷ Research

- ▷ From embedded to cloud-based Video Processing

▷ UTIA Results

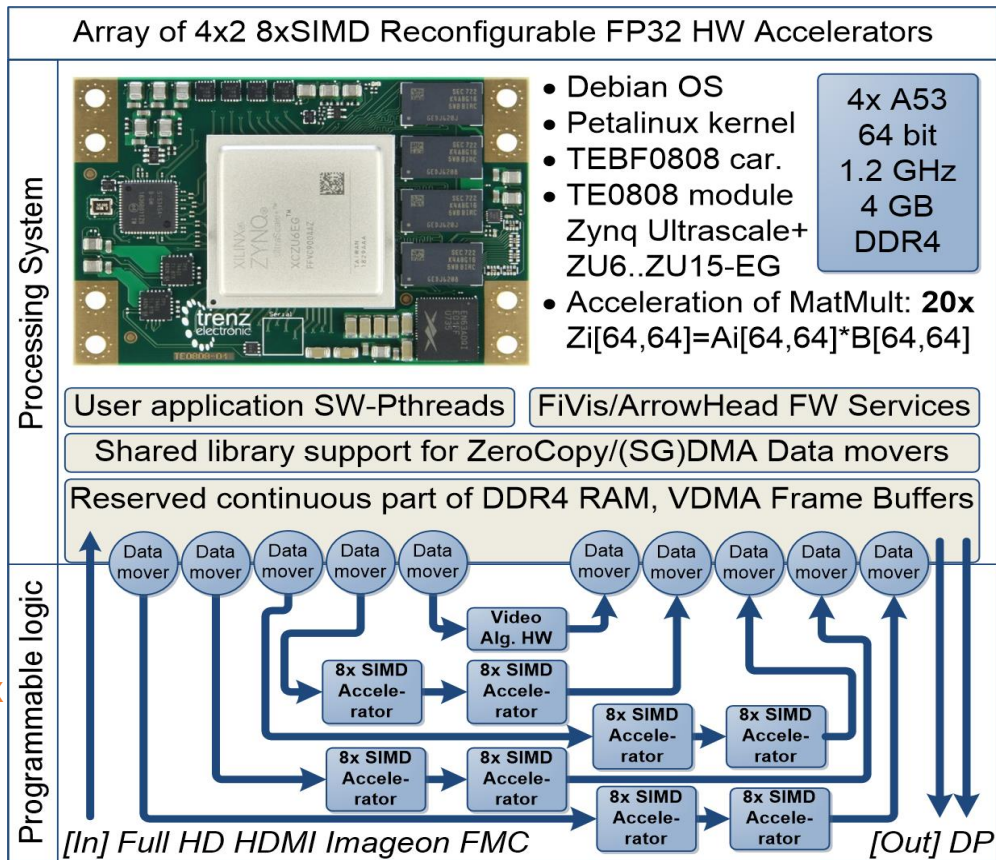
- ▷ Design time support for 28 nm Xilinx Zynq and 16 nm Zynq Ultrascale+ devices with Xilinx SDSoC C/C++ to HW system-level compiler.
- ▷ Support for UTIA 8x 8xSIMD FP FP32 reconfigurable HW accelerators

▷ Lucas Kanade Dense Optical Flow, SW/HW:

- ▷ Arm A53, 1.05 GHz SW:
0.1 FPS
- ▷ Zynq zu15-eg-1e 250 MHz HW:
60.0 FPS **600x**
- In paraleel with HW accelerated Matrix Multiplication FP32: **110x**

9 Eval. Packages:

<http://sp.utia.cz/index.php?ids=projects/fitoptivis>



FitOptiVis – Philips (NL), 30 partners

▷ Research

- ▷ From embedded to cloud-based Video Processing

▷ UTIA Results

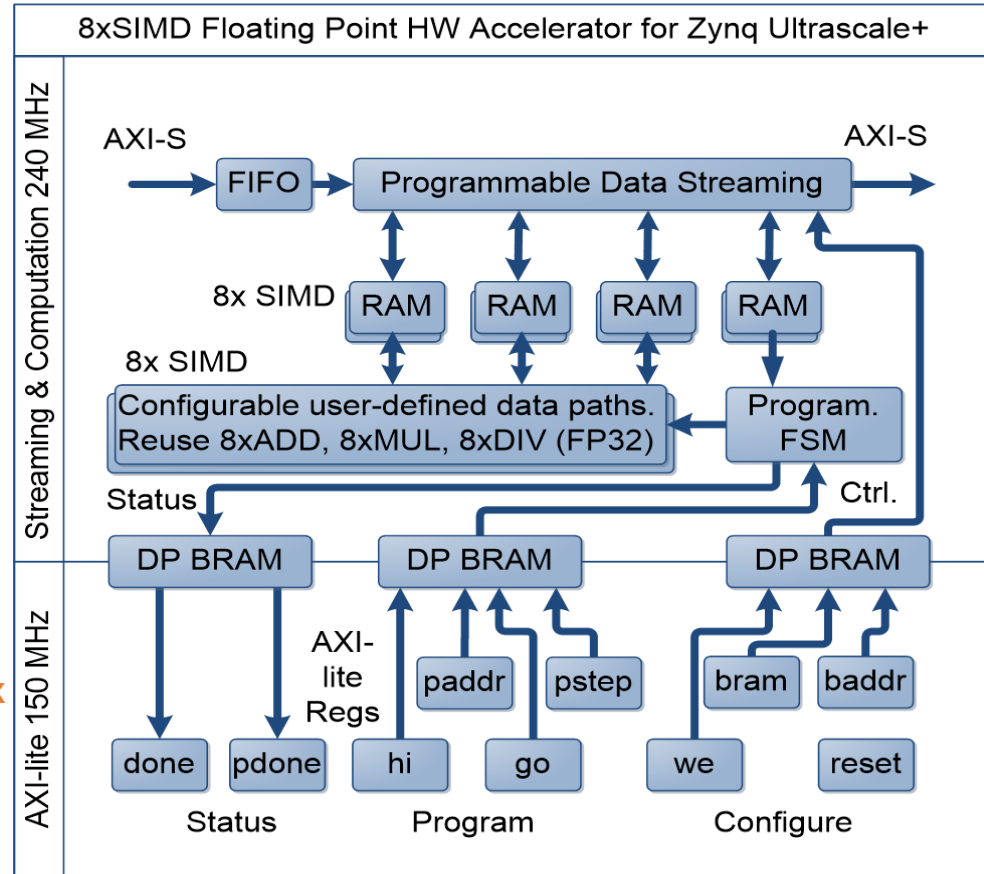
- ▷ Design time support for 28 nm Xilinx Zynq and 16 nm Zynq Ultrascale+ devices with Xilinx SDSoC C/C++ to HW system-level compiler.
- ▷ Support for UTIA 8x 8xSIMD FP FP32 reconfigurable HW accelerators

▷ Lucas Kanade Dense Optical Flow, SW/HW:

- ▷ Arm A53, 1.05 GHz SW:
0.1 FPS
- ▷ Zynq zu15-eg-1e 250 MHz HW:
60.0 FPS **600x**
- ▷ In paraleel with HW accelerated Matrix Multiplication FP32:
110x

9 Eval. Packages:

<http://sp.utia.cz/index.php?ids=projects/fitoptivis>



Arrowhead Tools – TU Lulea (S), 81 p.

▷ Research

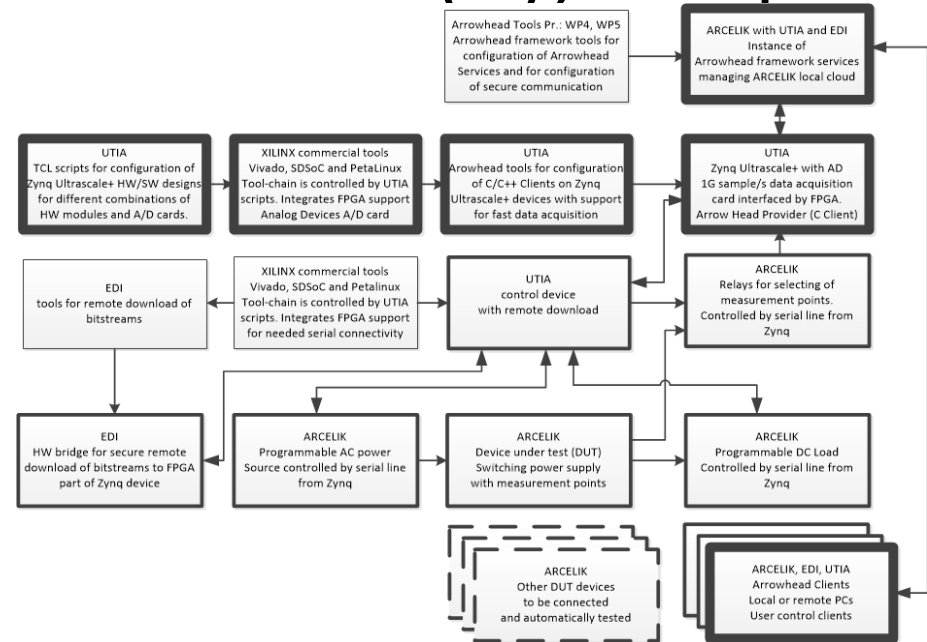
▷ Tools for systems of systems

▷ UTIA Results

- ▷ 2x 1G sample/s data acquisition for automated detection of errors of switching transistors in power supply units.
- ▷ Use Case: Tester of power-supply-units, for TVs for export to the Far-east.
- ▷ Partner company: Arcelik, Istanbul.
- ▷ Implementation of SW services for secure connectivity in a local cloud based on ArrowHead Framework middleware.

Project description:

<http://sp.utia.cz/index.php?ids=projects/ahtools>



Cooperation with ŠKODA AUTO a.s.

▷ **Research framework**

- ▷ **Framework agreement about realization educational activities between ŠKODA AUTO a.s. and ÚTIA AV ČR, v.v.i**

▷ **Research Topics**

- ▷ **Adaptive Decision-Making under Information Demanding Conditions**
- ▷ **Multiple Participant Decision Making**
- ▷ **Predictive Control for Industrial Robots**
- ▷ **Bayesian Approximate Recursive Identification and On-line Adaptive Control**
- ▷ **Learning Methods Applicable to Quantitative and Qualitative Data**
- ▷ **Multi-level Control of the Traffic in Large Urban Transportation Networks**
- ▷ **Modelling, Prediction and Simulation for Vehicle Systems for Assistance and Safety**

Cooperation with ŠKODA AUTO a.s.

▷ Research results

- ▷ Roboted autonomous driving (accelerator, brake, gear selector (floating)) on predefined circuit (length approx. 40 km) including development of HMI
- ▷ Regulator and „efficiency control model“ controls the accelerator, brake and gear selector to reach minimum consumption of energy
 - ▷ Optimal vehicle speed profile
 - ▷ HMI to assist the driver
 - ▷ Available energy management
- ▷ HW/SW subsystems for the autonomous parking



▷ Video 3:



Utia Autonomous Parking – Testing Presentation_0121_61s.mp4

Future projects with ŠKODA AUTO a.s.

- ▶ **USP - Urban Smart Park (EIT Urban Mobility)**
 - ▶ Urban Smart Park focusses on the development and pilot demonstration of automated vehicles that simplify driverless on-street inner-city parking.
 - ▶ <http://sp.utia.cz/index.php?ids=projects/usp>
- ▶ **TIE - Transportation Innovation Ecosystem (EIT UM)**
 - ▶ Creating a strategic infrastructure for urban policy management in the field of urban mobility. The overall objective is to define a set of policy recommendations provided to municipal leadership.
 - ▶ <http://sp.utia.cz/index.php?ids=projects/tie>
- ▶ **DTN – Doctorand Training Network (EIT UM)**
 - ▶ Doctorand longer-term research stays abroad.
 - ▶ <http://sp.utia.cz/index.php?ids=projects/dtn>
- ▶ **Other HW systems with our SW support.**
 - ▶ <http://sp.utia.cz/index.php?ids=results>

VIDEO 4:

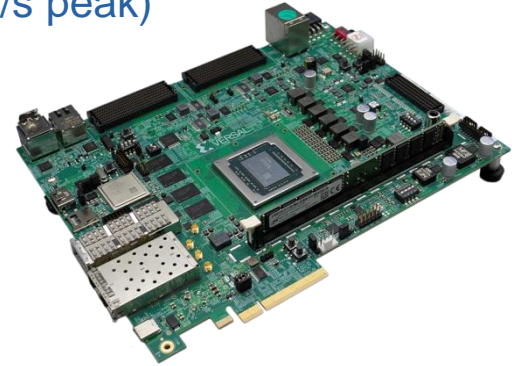


Future Extern Funding

		2020	2021	2022	2023	2024
SILENSE	(ECSEL JU)	■	■			
PRODUCTIVE 4.0	(ECSEL JU)	■	■	■		
WAKEMEUP	(ECSEL JU)	■	■	■	■	■
FITOPTIVIS	(ECSEL JU)	■	■	■	■	■
ARROWHEAD TOOLS	(ECSEL JU)	■	■	■	■	■
STORAIGE	(ECSEL JU)			■	■	■
DTN	(EIT Urban Mobility)	■	■	■	■	■
TIE	(EIT Urban Mobility)	■	■	■	■	■
USP	(EIT Urban Mobility)	■	■	■	■	■
External funding ECSEL (Mil Kč)		8,934	8,672	5,491	4,000	2,000
External funding ECSEL 2020-24		29,097 Mil Kč = 1,077 Mil €				

Future of the team 2020 – 2024

- ▶ In 2021, Department have invested into this 7nm Equipment:
 - ▶ Versal ACAP AI Core Series VCK190 (400 GPU, 10 TFLOP/s peak)
 - ▶ Versal ACAP Prime Series VMK180
- ▶ We plan to build on our current strengths:
 - ▶ Design of custom board support packages for advanced computing architectures targeting single-chip, HW-accelerated DSP aps.
 - ▶ IP design for SoCs with FPGA. UTIA licensed IPs.
 - ▶ Mapping of recursive DSP/AI/ML algorithms to HW (StorAlge proj.).
 - ▶ Design of normalized, QR DSP fixed-point algorithms as HW IPs.
 - ▶ Clustering/Classification by recursive mixture estimation as HW IPs.
 - ▶ Teaching of Bc/MSc/PhD students at the CTU, Faculty of Transport.
 - ▶ New concepts of HMI systems in cooperation with Skoda Auto a.s.



Thank you for your attention.