Application Note

Akademie věd České republiky
Ústav teorie informace a automatizace AV ČR, v.v.i.

Toshiba Video Sensor Evaluation Platform for TE0720-03-2IF SoM on TE0701-05 Carrier

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Revision history:

Rev.	Date	Author	Description
1	05.07.2016	Jiří Kadlec	Evaluation package for Xilinx SDK 2015.4
2	18.07.2016	Jiří Kadlec	SD cards with compiled SDSoC SW projects

Acknowledgements:

This work has been partially supported by:
ARTEMIS JU project ALMARVI No. 621439 and by related MEYS (CZ NFA) project 7H14004.

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1. Summary

1.1 Key features

This application note describes HW platform performing edge detection and motion detection video processing for Toshiba Full HD colour video sensor with fixed resolution (1920x1080p60).

Arm Cortex A9 processor of Xilinx Zynq is performing initialisation and synchronisation of the video processing chain. Program and the FPGA image is downloaded to the board from the Xilinx SDK 2015.4 via USB JTAG to the 1GB DDR3 located on the Zynq system on module. System can be also started directly from the SD card. Arm processor initiates the IP cores in the programmable logic (PL) part of the Zynq. It also initiates the Toshiba video sensor and the video output to the Full HD monitor with fixed 1920x1080p60 resolution.

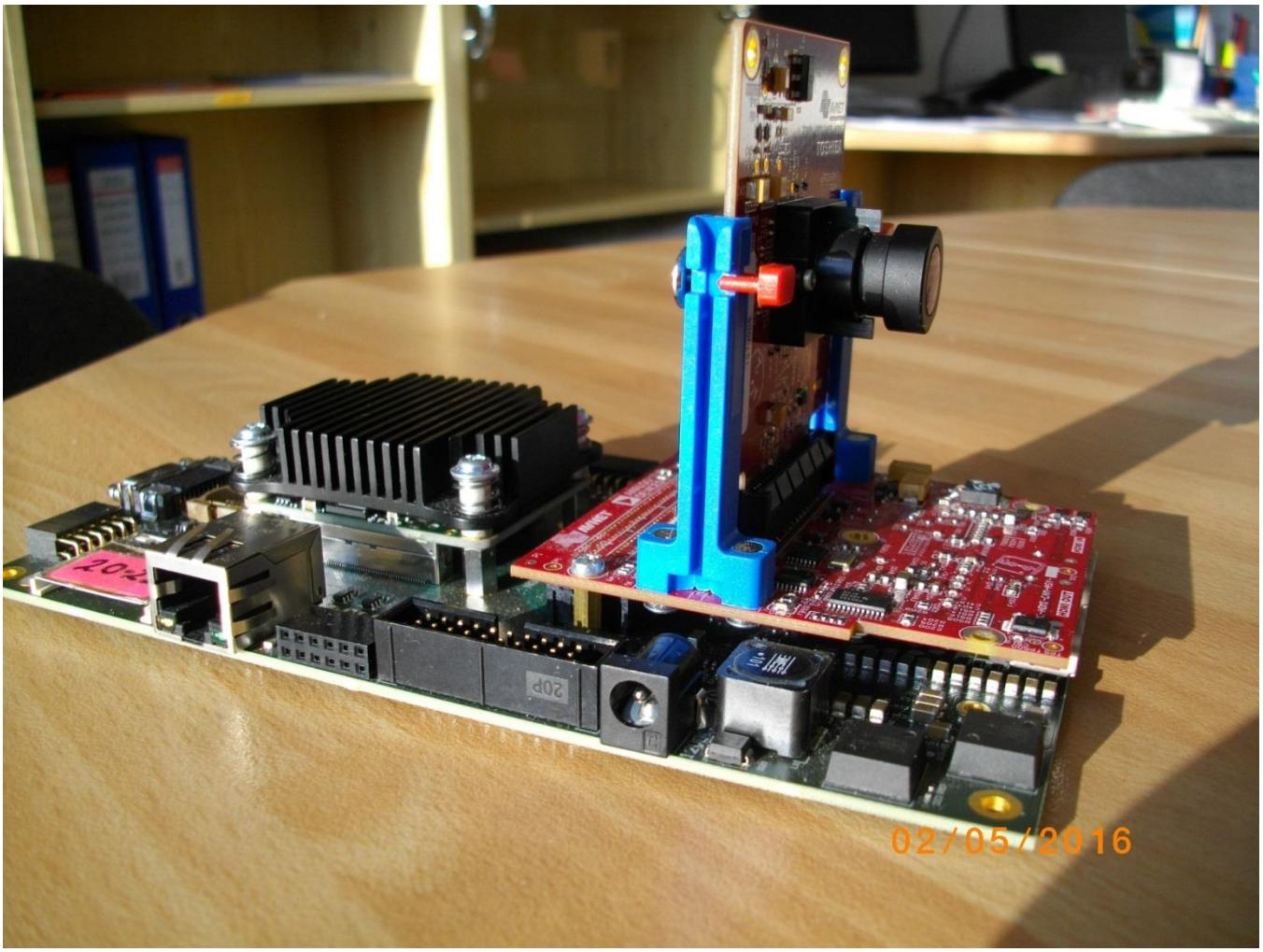


Figure 1: Toshiba Full HD evaluation platform HW.

- Raw video data are provided by the Toshiba video sensor.
- Data are processed into the YCrCb 16 bit per pixel format and stored by Video DMA (VDMA) to input video frame buffers (VFBs) defined in the DDR3.
- HW DMA controller(s) send data from the input VFBs to the processing accelerators in PL.
- Another DMA controller(s) send processed data from HW to the output VFBs in DDR3.
- Second part of the VDMA is sending data to the Full HD display.

1.2 Project sh01: Edge detection with single HW accelerator

Zynq module:	TE0720-02-2IF (Trenz)
Carrier board:	TE701-05 (Trenz)
FMC Interface:	BD-FMC-HDMI-CAM-G (Avnet)
FMC card input:	Full HD Toshiba video sensor (1080p60)
FMC card output:	Full HD HDMI output to display (1080p60)
Accelerator:	None.
Platform:	C:\S\t20i2t1\hio
Demos(SDK2015.4):	C:\VM07\t20i2t1\sh01_rows_resize_25_to_100.c C:\VM07\t20i2t1\sh01_rows_fixed_100.c

Design by UTIA in Xilinx SDSoC 2015.4. Date: 2016_05_27

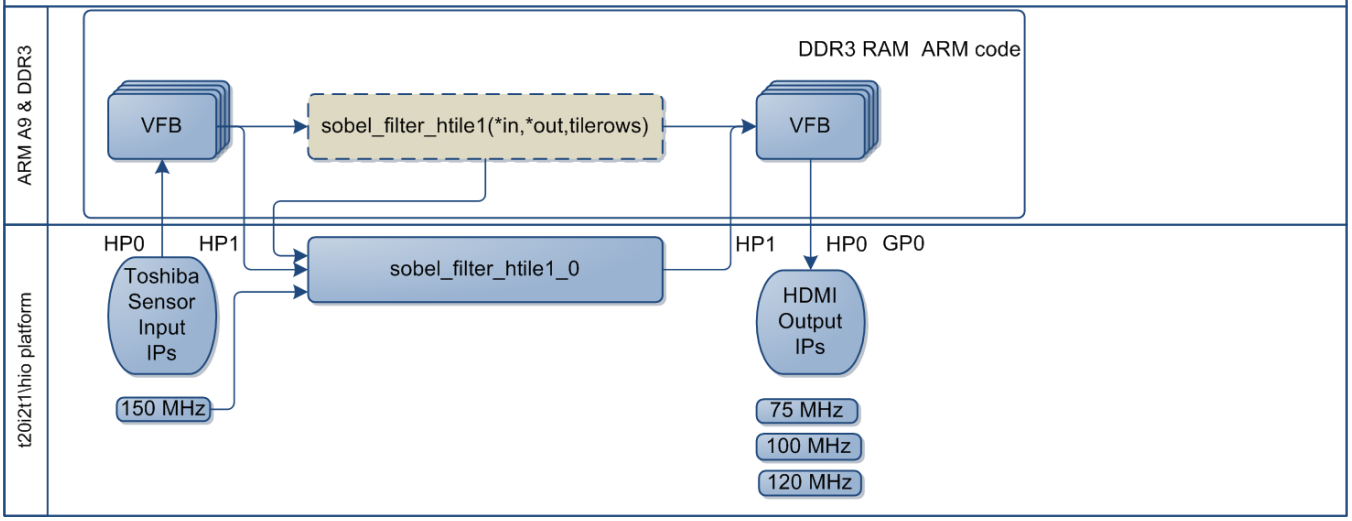
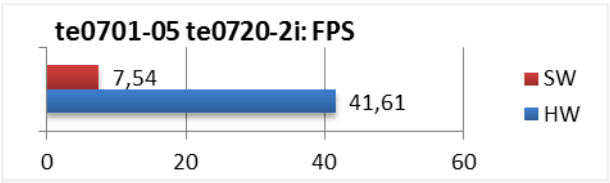
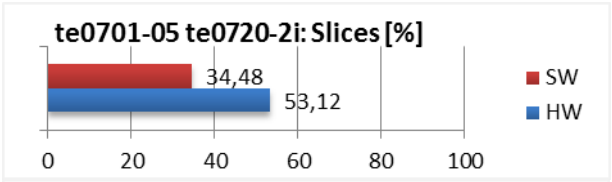
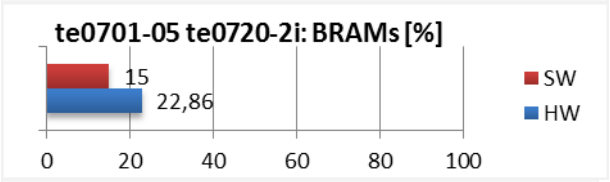


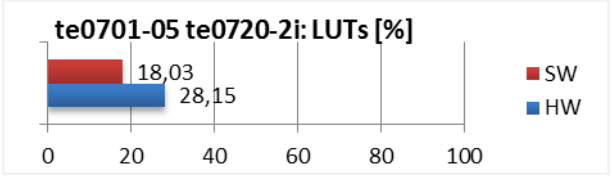
Figure 2: Project sh01 - Edge detection with single HW accelerator

TE0720-02-2IF Sobel 1x
Energy per one frame (SW): 1004.3 mJ
Energy per one frame (HW): 183.1 mJ
Energy per frame reduction: **5.48 x**









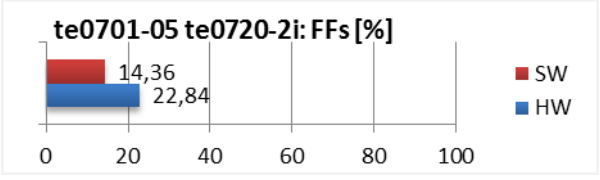


Figure 3: Project sh01 - Energy per frame reduction and used HW resources.

1.3 Project sh02: Edge detection with two HW accelerators

Zynq module:	TE0720-02-2IF (Trenz)
Carrier board:	TE701-05 (Trenz)
FMC Interface:	BD-FMC-HDMI-CAM-G (Avnet)
FMC card input:	Full HD Toshiba video sensor (1080p60)
FMC card output:	Full HD HDMI output to display (1080p60)
Accelerator:	None.
Platform:	C:\S\t20i2t1\hio
Demos(SDK2015.4):	C:\VM07\t20i2t1\sh02_rows_resize_25_to_100.c C:\VM07\t20i2t1\sh02_rows_fixed_100.c

Design by UTIA in Xilinx SDSoC 2015.4. Date: 2016_05_27

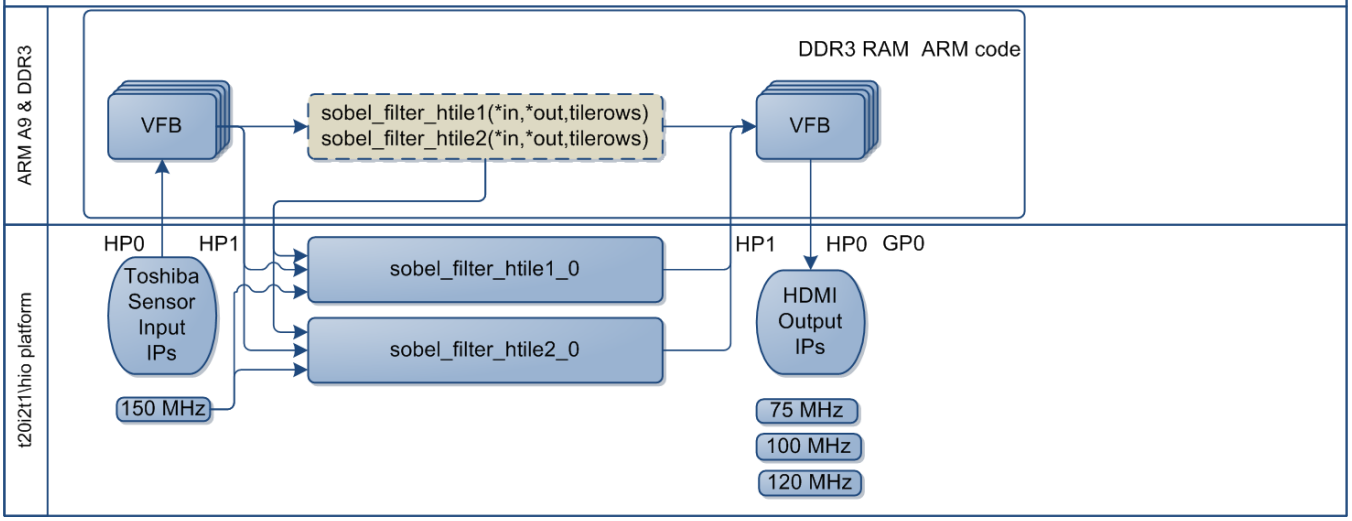
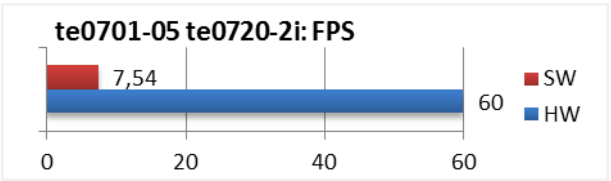
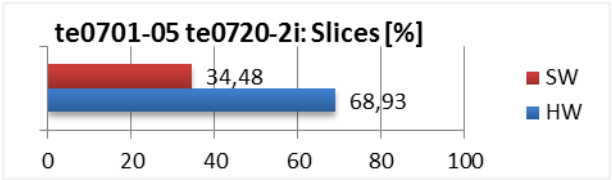
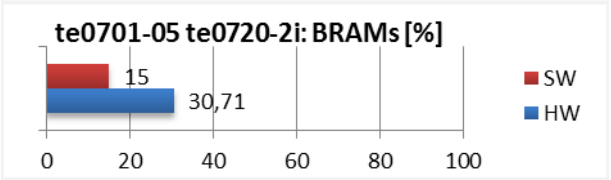


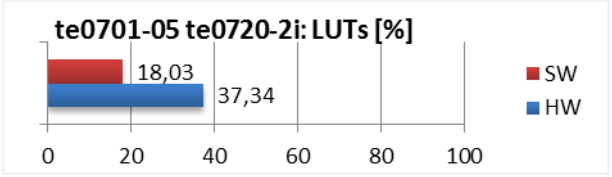
Figure 4: Project sh02 - Edge detection with two HW accelerators

TE0720-02-2IF Sobel 2x
Energy per one frame (SW): 1001.6 mJ
Energy per one frame (HW): 129.4 mJ
Energy per frame reduction: **7.74 x**









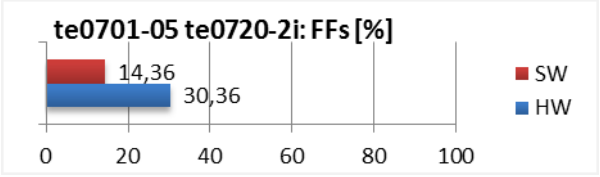


Figure 5: Project sh02 - Energy per frame reduction and used HW resources.

1.4 Project sh03: Edge detection with three HW accelerators

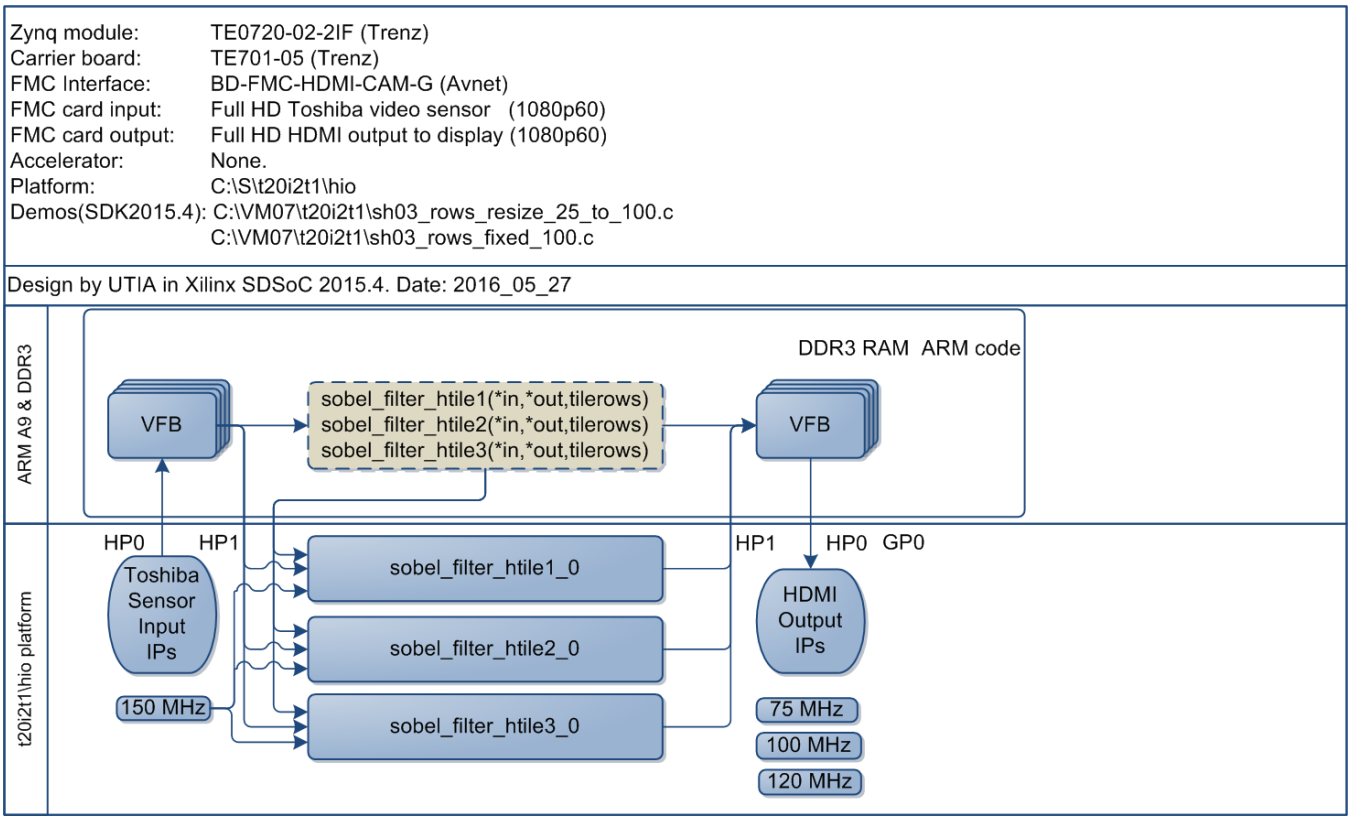
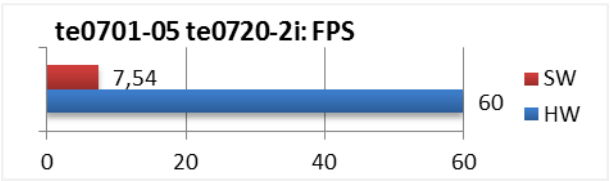
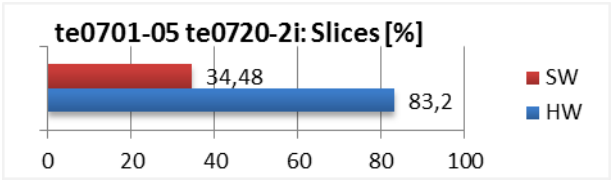
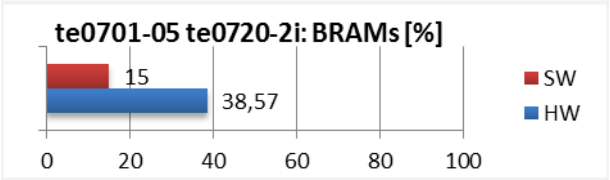


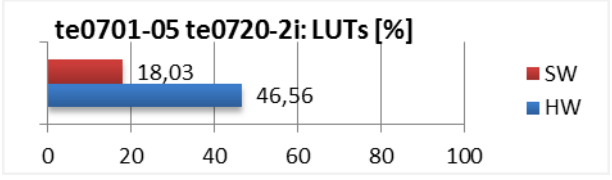
Figure 6: Project sh03 - Edge detection with three HW accelerators

TE0720-02-2IF Sobel 3x
Energy per one frame (SW): 1039.0 mJ
Energy per one frame (HW): 130.8 mJ
Energy per frame reduction: **7.94 x**









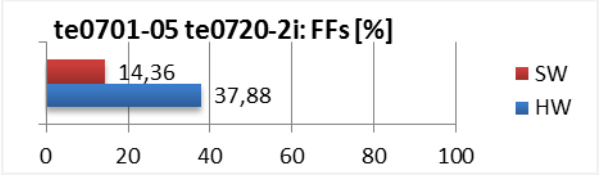


Figure 7: Project sh03 - Energy per frame reduction and used HW resources.

1.5 Project md01: Motion detection with single chain of HW accelerators

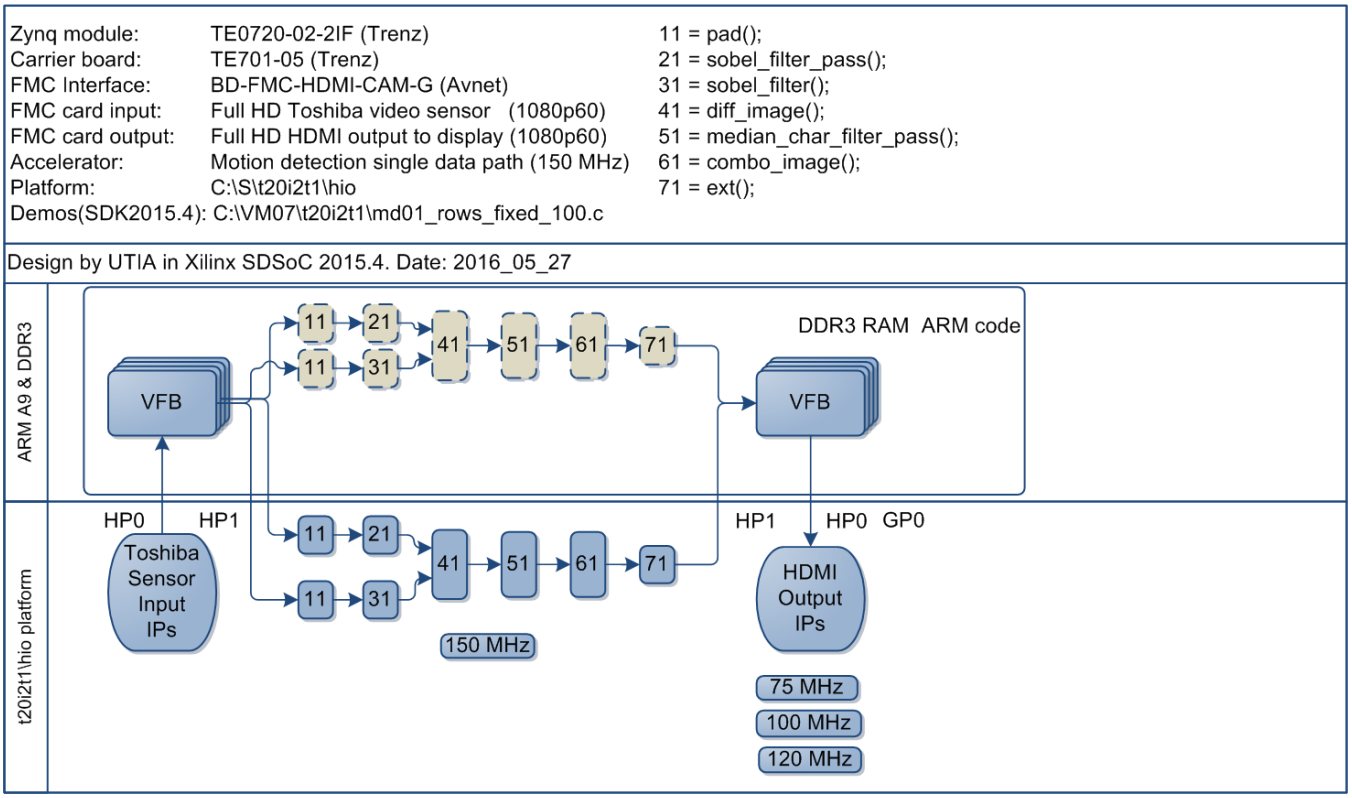
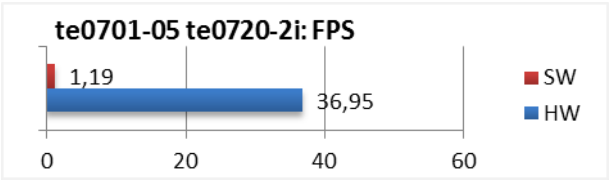
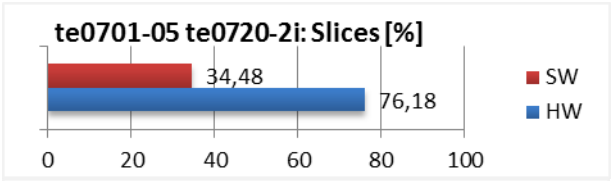
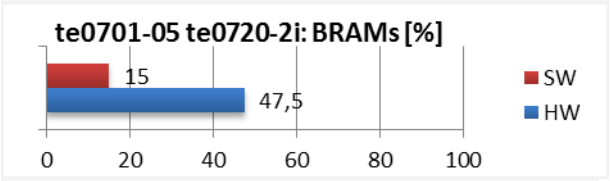


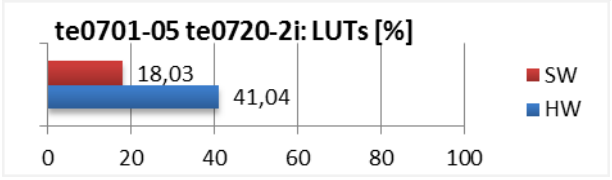
Figure 8: Project md01 - Motion detection with single HW accelerator data path

TE0720-02-2IF Motion Detection 1x
Energy per one frame (SW): 6453.8 mJ
Energy per one frame (HW): 217.3 mJ
Energy per frame reduction: **29.7 x**









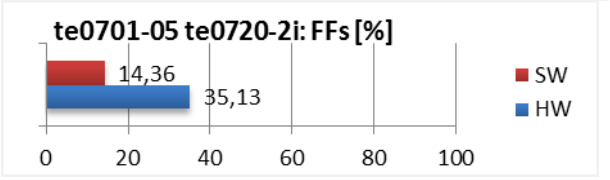


Figure 9: Project so01 - Energy per frame reduction and used HW resources.

1.6 Project md02: Motion detection with two chains of HW accelerators

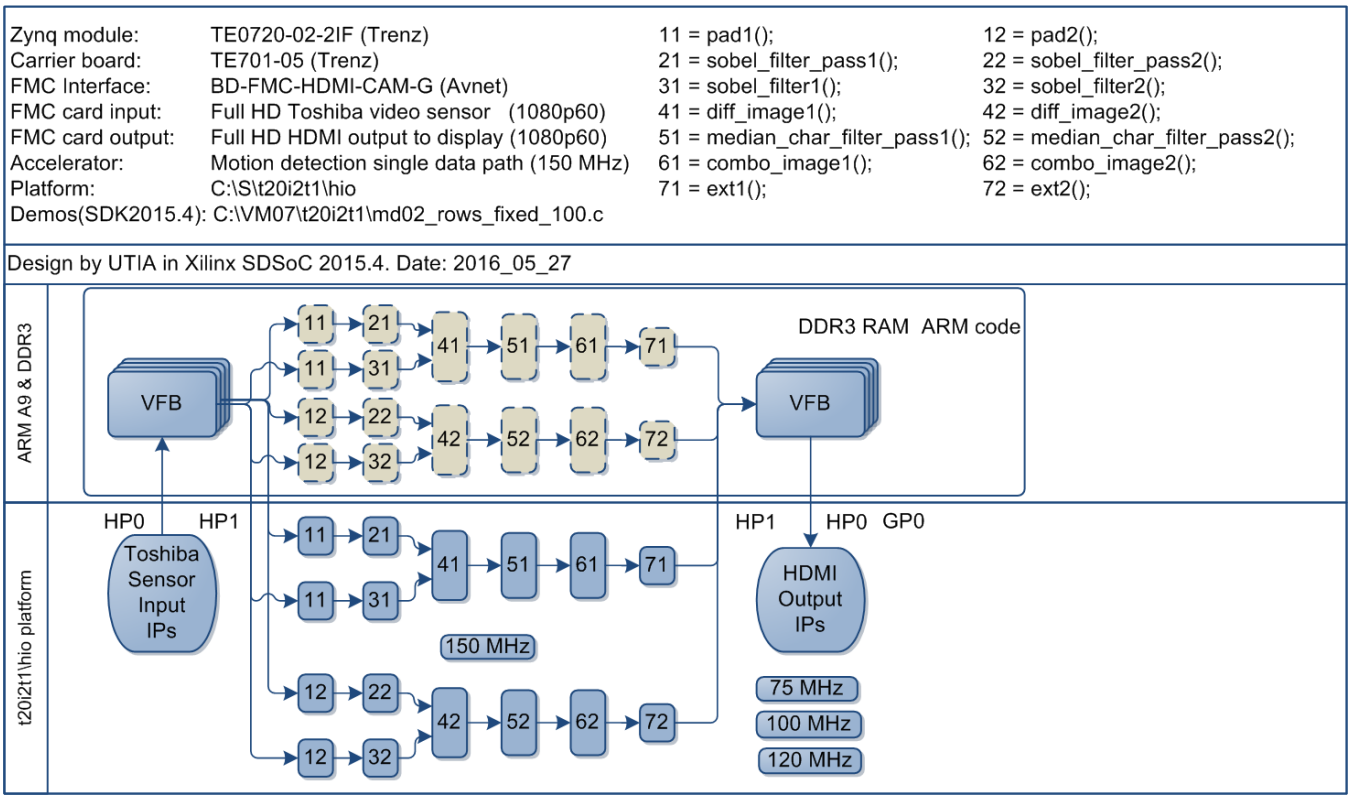
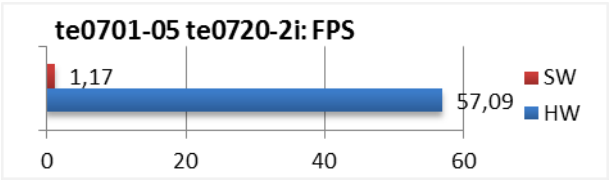
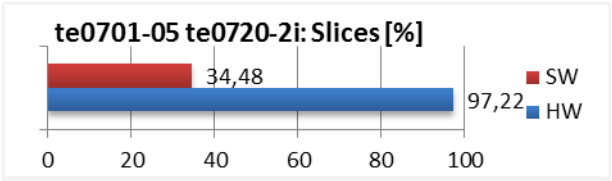
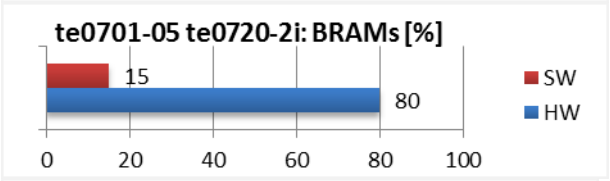


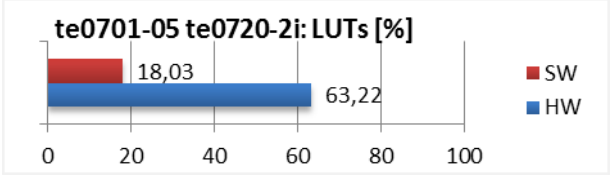
Figure 10: Project md02 - Motion detection with two HW accelerator data paths

TE0720-02-2IF Motion Detection 2x
Energy per one frame (SW): 6584.6 mJ
Energy per one frame (HW): 147.1 mJ
Energy per frame reduction: **44.76 x**









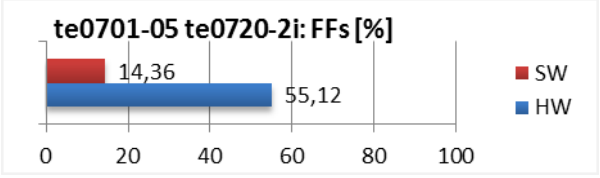


Figure 11: Project so02 - Energy per frame reduction and used HW resources.

2. Installation of evaluation package

2.1 Import of SW projects in Xilinx SDK 2015.4

Unzip the evaluation package to directory of your choice.
The directory **C:\VM_07** will be used in this application note.
C:\VM_07\t20i2t1_V54_IMPORT

Create empty directory for Xilinx SDK workspace.
C:\VM_07\t20i2t1

Start Xilinx SDK 2015.4 and select the directory for the SDK 2015.4 workspace. See Figure 12. Select **C:\VM_07\t20i2t1**

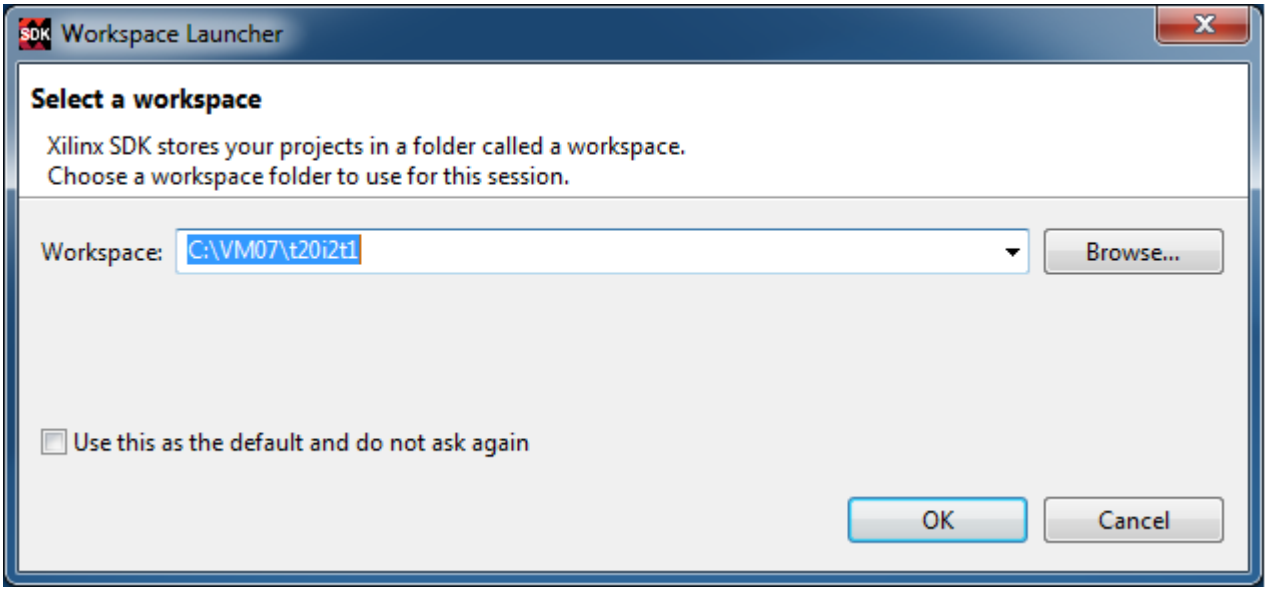


Figure 12: Select the SDK Workspace

HW and SW projects can be imported into SDK now. Select:

File -> Import -> General -> Existing Projects into Workspace
Click on Next button. See Figure 13.

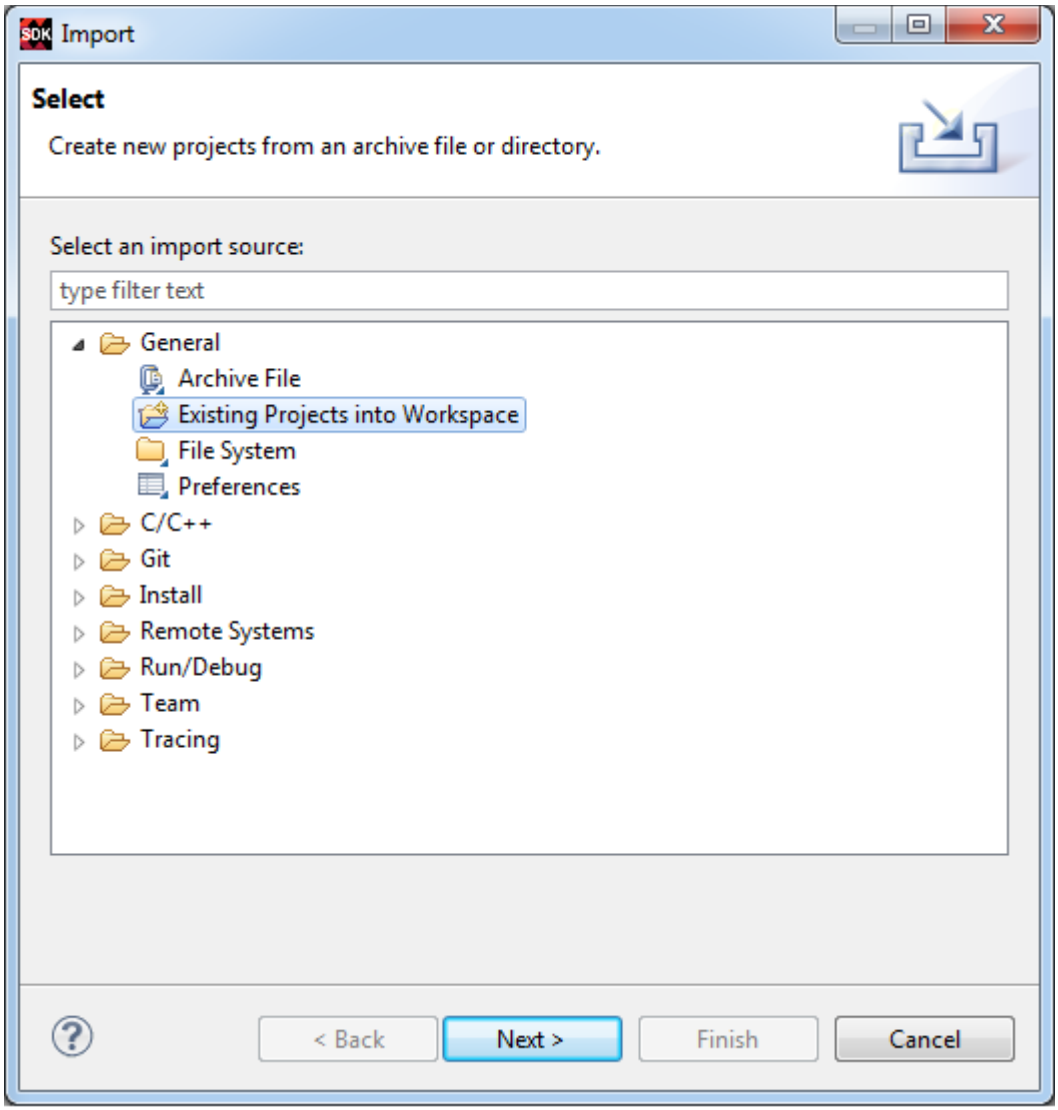


Figure 13: Import Existing Projects into Workspace

Type directory with projects to be imported. See Figure 14.

C:\VM_07\t20i2t1_V54_IMPORT

Set the "**Copy projects into workspace**" check box.
Click on Finish button. See Figure 14.

Process of compilation will start automatically. This first compilation of all SDK SW projects can take several minutes to finish. It should finish without errors.

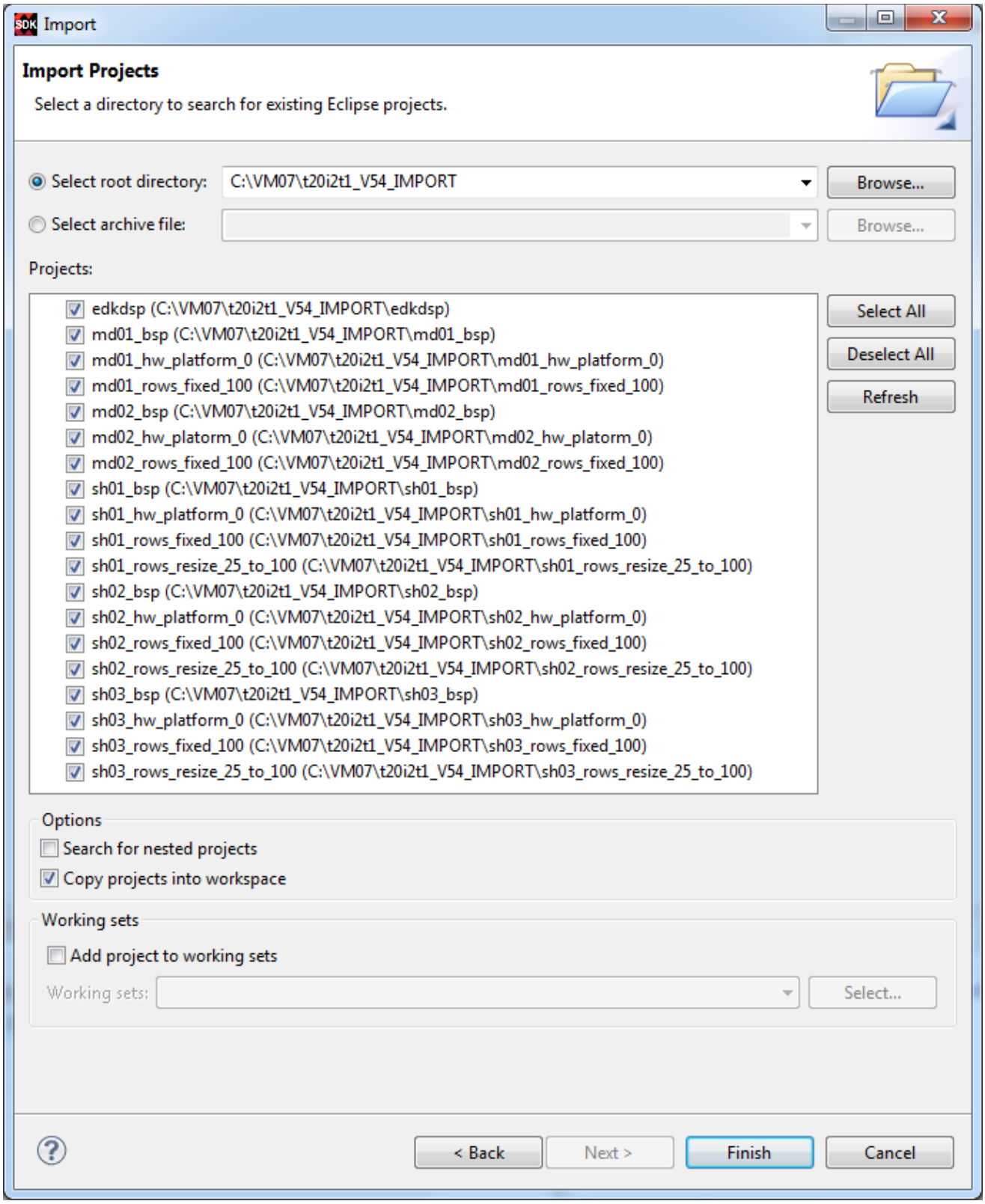


Figure 14: Select "Copy projects into workspace" and finish the import of all projects.

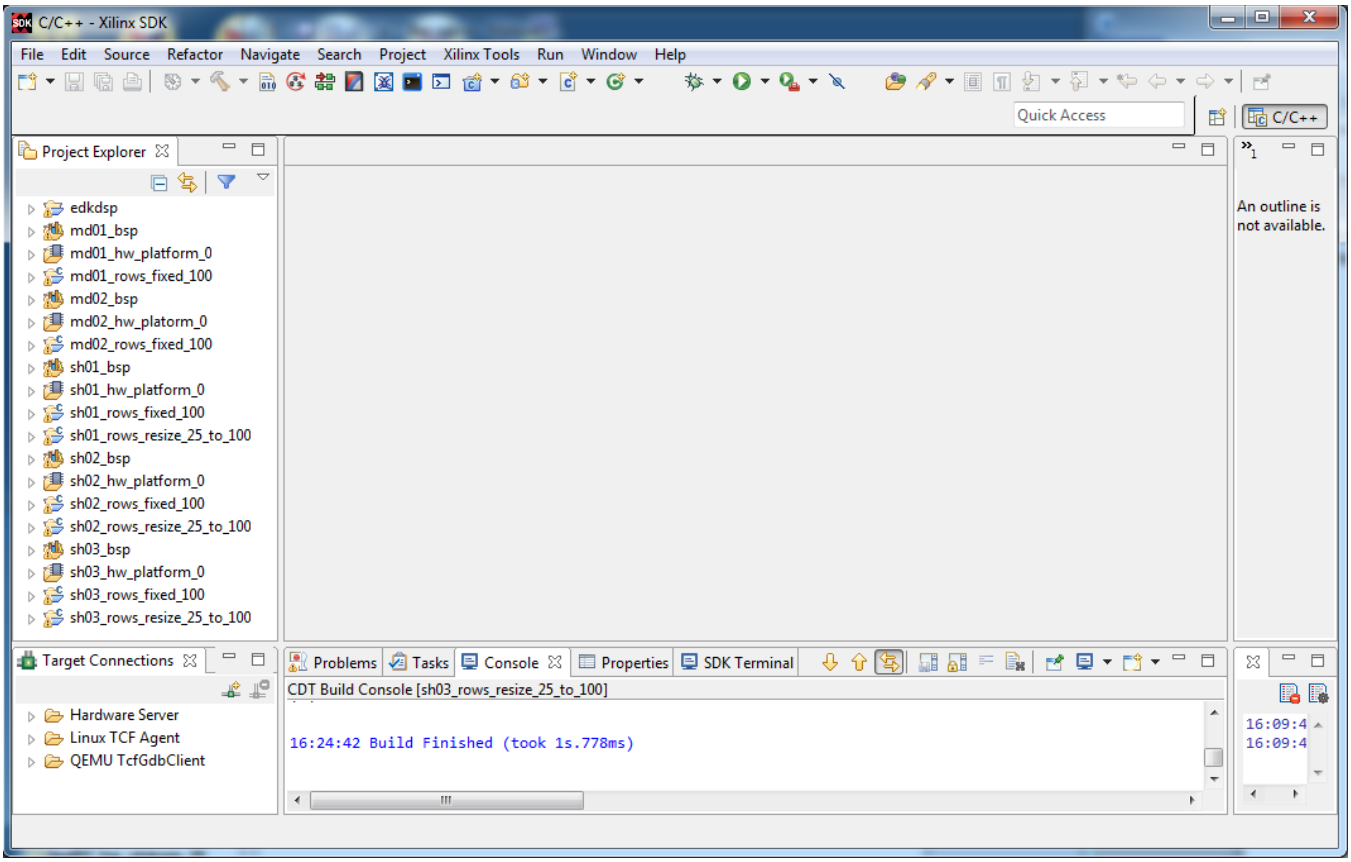


Figure 15: All projects are compiled in debug mode.

SDK 2015.4 compiles SW of all imported demos in debug mode.

2.2 HW setup

HW setup is using commercially accessible components [1], [2], [3], [4], [5]:

TE0720-03-2IF; Part: XC7Z020-2CLG484I; 1 GByte DDR; Industrial Grade;	Price: €269,00 [1]
Heatsink for TE0720, spring-loaded embedded;	Price: €19.00 [2]
TE0701-05 Carrier Board for Trenz Electronic 7 Series;	Price: €249.00 [3]
AES-FMC-HDMI-CAM-G FMC card with HDMI I/O and CAM interface	Price: $250.00 [4]
Toshiba Industrial 1080P60 Camera Module	Price $229.00 [5]

HW Options:

TE0720-03-2IF	can be replaced by	**TE0720-02-2IF**	(Same Price, both boards from Trenz) [1].
TE0701-05	can be replaced by	**TE0701-04**	(Same Price, both boards from Trenz) [3].

Trenz TE0701-04 or TE0701-05 carriers require modifications to run the FMC Imageon carrier AES-FMC-HDMI-CAM-G with Zynq TE0720-03-2IF system on module. The modification is related to the swapped polarity of the differential clock signal for the FMC board. Evaluation HW systems with carriers TE0701-04 or TE0701-05 provided by UTIA have these modifications already done.

UTIA can implement these HW modifications for the original Trenz TE0701-04 and TE0701-05 carriers. This requires written e-mail request to kadlec@utia.cas.cz . Request will be first confirmed by UTIA. The interested party has to cover the cost of shipment of the carrier board to/from UTIA. Modification can be done in 5 working days and it is offered free of charge.

2.3 Test demos

To test demos follow these steps:

- Insert the Toshiba Full HD video sensor to the connector on the Imageon board.
- Connect Full HD (or DVI) monitor by HDMI cable to the HDMI OUT on the Imageon FMC card.
- Switch the monitor ON.
- Connect the carrier board by USB-to-microUSB cable to PC to support JTAG serial link and the standard serial terminal.
- Connect power supply (DC 12V).
- Open and configure the standard serial terminal client (PuTTY or similar) on PC.
  (Speed: 115200 baud; Data bits: 8; Stop bits: 1; Parity: None; Flow control: None.)
- Reset the board. Board will start first stage boot loader from internal flash as set up by Trenz. It is writing messages to the serial terminal. On request, “Hit any key to stop autoboot” type any key to stop the auto-boot of linux.
- If you need to switch-off the power, close first the serial terminal on the PC. This will help to avoid problems

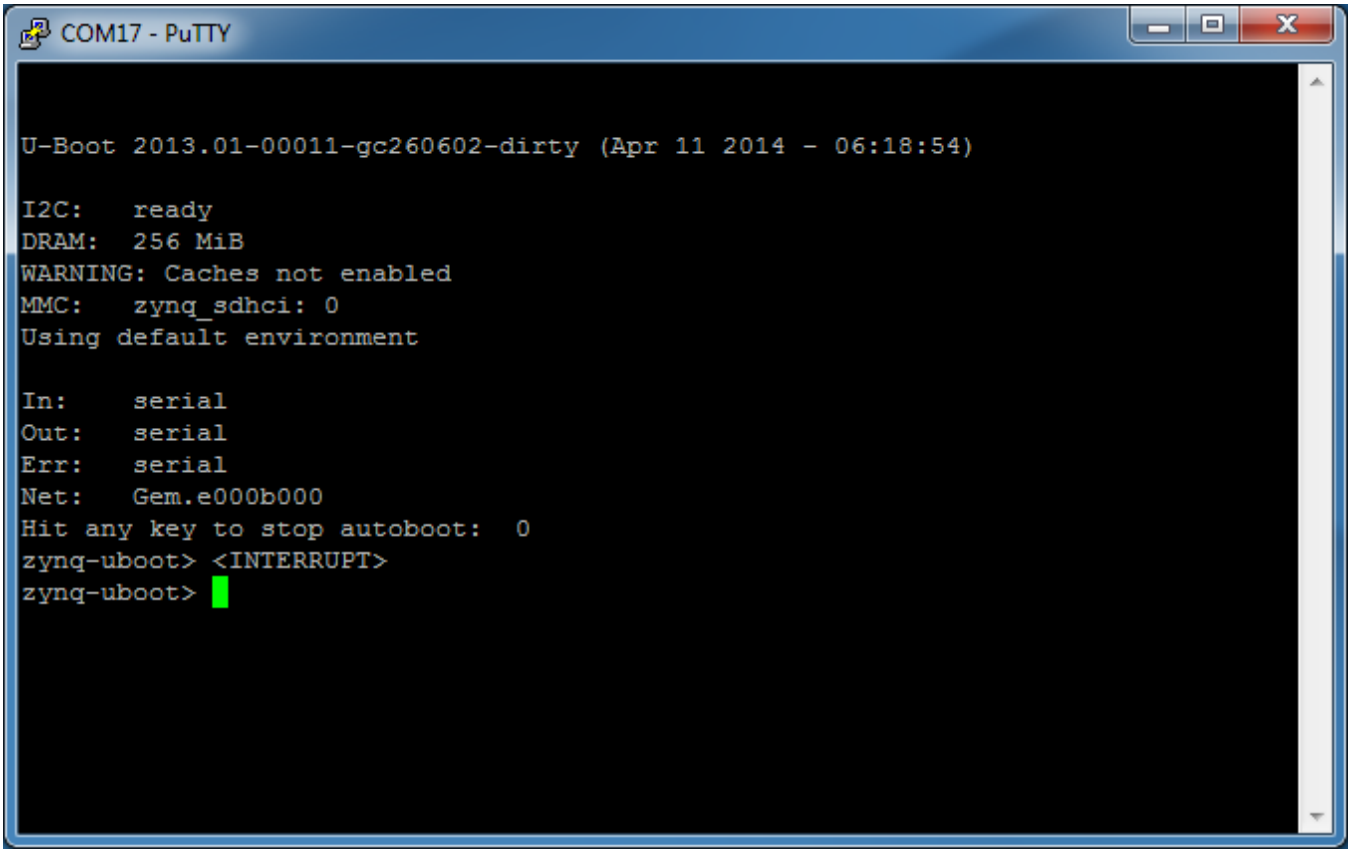


Figure 16: Serial console. Reset board and stop autoboot.

Download bitstream to the board. Demo **sh01_rows_fixed_100** will be used as an example.
The **bitstream.bit** for demo **sh01** is located in the directory:

C:\VM_07\t20i2t1\sh01_hw_platform_0

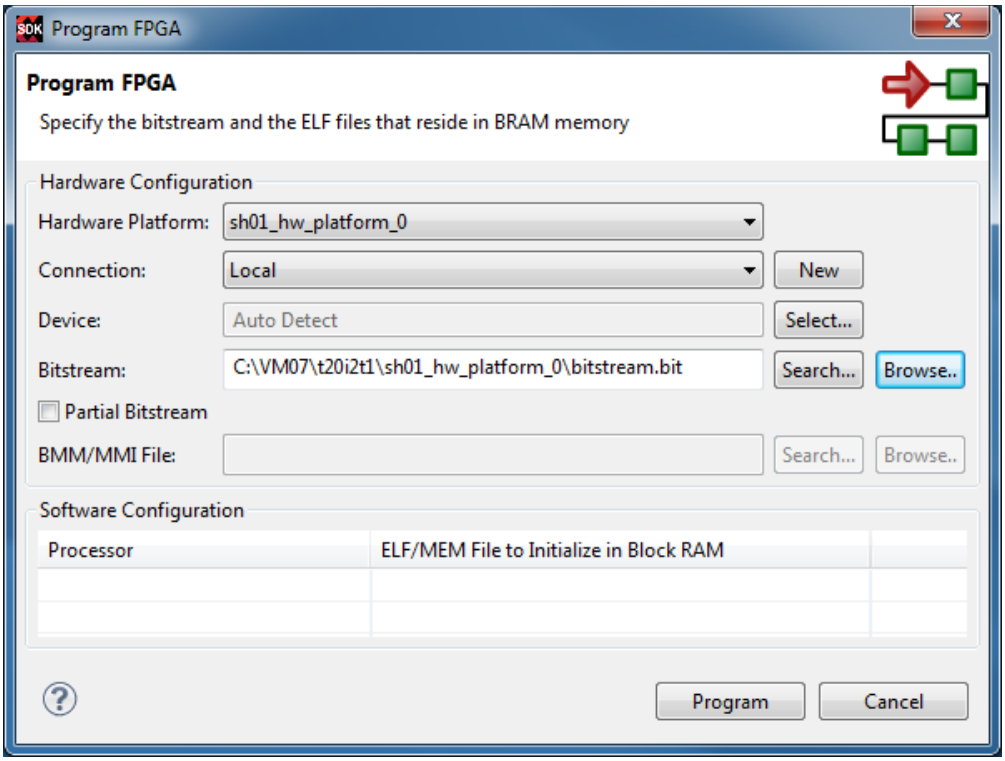


Figure 17: Download bitstream to the PL part of Zynq.

Select Program to download the bitstream to the PL part of Zynq via the USB cable in JTAG mode.

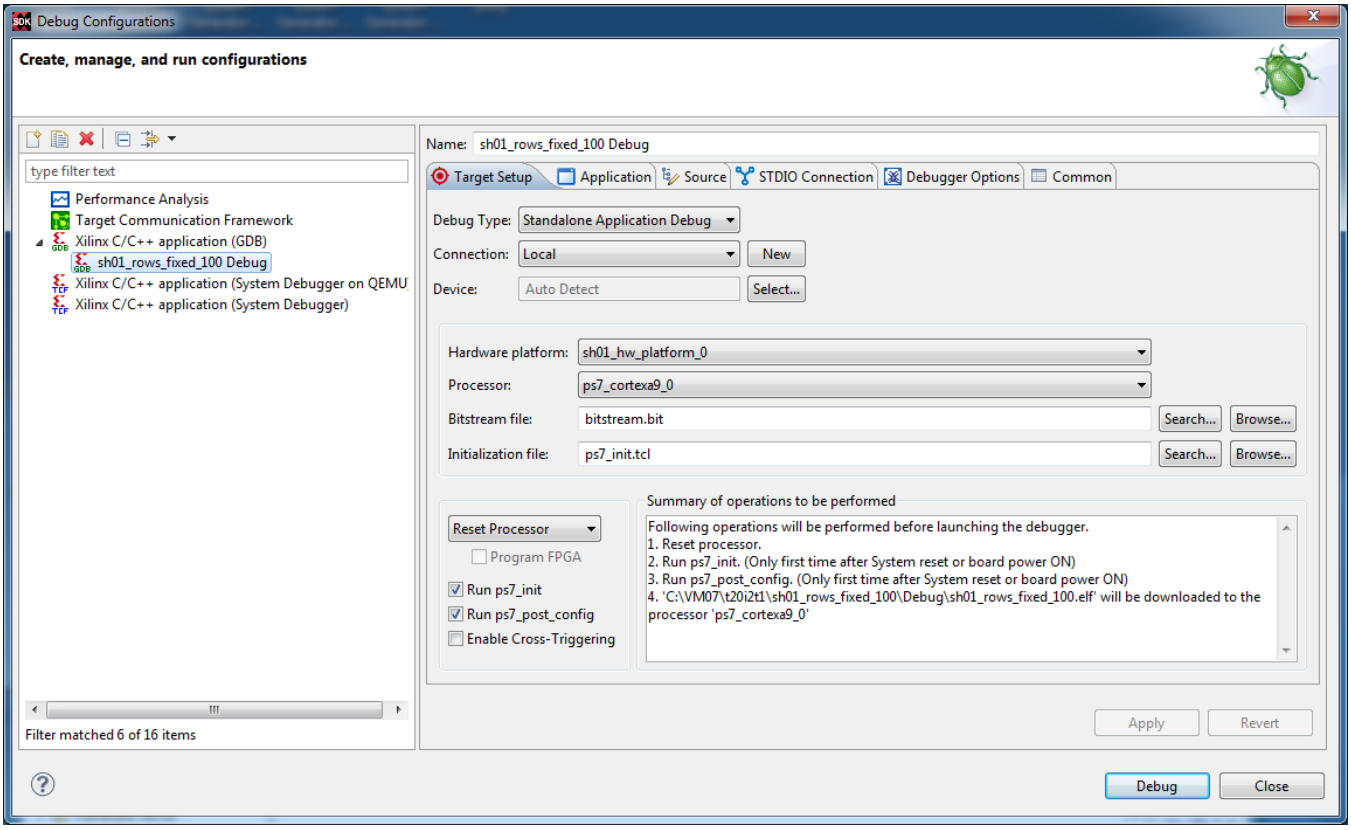


Figure 18: Select demo application for debug.

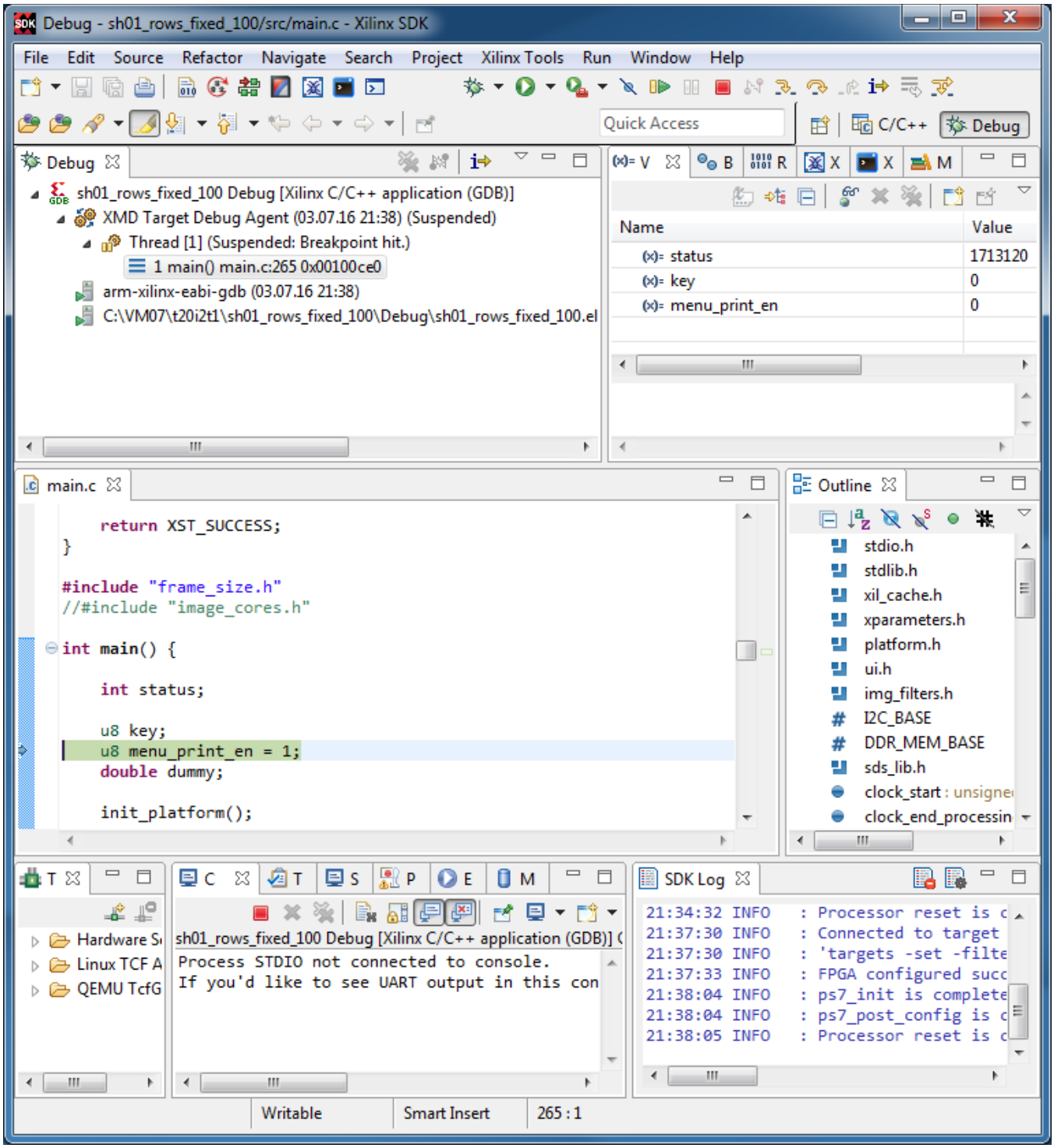


Figure 19: Debug stops at first executable line of Arm Cortex A9 code.

- All evaluation demos can be also compiled into Release versions with optimisation set to -O2 or -O3.
- All evaluation demos can boot directly from SD card. FSBL projects can use the standard project template as provided by the SDK 2015.4
- Demo **sh01_rows_fixed_100** works on complete frame with single HW accelerator data path
- Demo **sh01_rows_resize_25_to_100** works with identical HW. But SW scales dynamically the number of lines to be processed. This is scaling from ¼ of frame to the complete frame. Part of the frame which is not processed is automatically propagating the input video signal via the cyclic structure of 8 video frame buffers. The HW data movers are instructed about the number of lines to be processed. SW is writing this information to an AXI-lite configuration register of the data mover IP core.
- Demos **sh02_rows_fixed_100** and **sh02_rows_resize_25_to_100** work with 2 data paths.
- Demos **sh03_rows_fixed_100** and **sh03_rows_resize_25_to_100** work with 3 data paths.
- Demos **md01_rows_fixed_100** and **md02_rows_fixed_100** work with one and two HW video processing chains. These HW chains have only fixed set of processed lines (1x 100% and 2x 50% of the frame).

Files for the SD card (SW implementation of video processing algorithms on Arm in SDSoC 2015.4) can be found in:

SD_cards\SW\sh01\BOOT.bin
SD_cards\SW\sh02\BOOT.bin
SD_cards\SW\sh03\BOOT.bin
SD_cards\SW\md01\BOOT.bin
SD_cards\SW\md02\BOOT.bin

These files can be used for evaluation of the system performance in case of sequential SW computation on Arm Cortex A9 processor without HW acceleration. Projects have been compiled with maximal optimisation (-O3) without use of NEON.

3. References

[1] TE0720-03-2IF; Part: XC7Z020-2CLG484I; 1 GByte DDR; Grade: Industrial; Price: €269,00.
http://shop.trenz-electronic.de/en/TE0720-03-2IF-Xilinx-Zynq-module-XC7Z020-2CLG484I-ind.-temp.-range-1-Gbyte

[2] Heatsink for TE0720, spring-loaded embedded; Price: €19.00.
https://shop.trenz-electronic.de/en/26922-Heatsink-for-TE0720-spring-loaded-embedded?c=38

[3] TE0701-05 Carrier Board for Trenz Electronic 7 Series; Price: €249.00.
https://shop.trenz-electronic.de/en/TE0701-05-Carrier-Board-for-Trenz-Electronic-7-Series

[4] AES-FMC-HDMI-CAM-G Price: $250.00.
http://products.avnet.com/shop/en/ema/3074457345623664802

[5] Toshiba Industrial 1080P60 Camera Module; Price $229.00.
http://zedboard.org/sites/default/files/product_briefs/PB-AES-CAM-TOSH-1080P-G-v5-web.pdf

4. Evaluation license

The **evaluation version of the package** can be downloaded from UTIA www pages free of charge for evaluation of HW accelerated edge detection and motion detection algorithms for the Toshiba Full HD video sensor on TE0720-03-2IF module [1] located on TE0701-05 carrier [3].

The evaluation package includes SDK 2015.4 SW projects with C source code for Arm Cortex A9 processor (32bit) in standalone mode.

The evaluation package includes these static libraries for Arm Cortex A9 processor (32bit) for standalone mode:

libfmc_imageon.a	SDK 2015.4 UTIA static library with interface functions for video IP cores
libsh01.a	SDSoC 2015.4 static library for HW accelerator in project sh01
libsh02.a	SDSoC 2015.4 static library for HW accelerator in project sh02
libsh03.a	SDSoC 2015.4 static library for HW accelerator in project sh03
libmd01.a	SDSoC 2015.4 static library for HW accelerator in project md01
libmd02.a	SDSoC 2015.4 static library for HW accelerator in project md02

These libraries have no time restriction.
Source code of these libraries is not provided in this evaluation package.

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