Application Note

Akademie věd České republiky
Ústav teorie informace a automatizace AV ČR, v.v.i.

SDSoC 2015.4 Standalone BSP with Full HD HDMI In-Out SW and HW Demos for Zynq System-on-Module TE0720-03-2IF and TE0701-05 Carrier Board

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Revision history:

Rev.	Date	Author	Description
1	15.08.2016	Jiří Kadlec	BSP for SDSoC 2015.4 on Trenz TE0701-05 carrier board with TE0720-03-2IF Zynq SoM. Description of installation and use of the BSP.

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1. Summary

1.1 Introduction

This application note describes installation and use of a **stand-alone board support package (BSP) for the Xilinx SDSoC 2015.4 for the Trenz TE0701-05 platform [3] with industrial grade Zynq XC7Z020-2CLG484I device on System on Module TE0720-03-2IF [1].**

This stand-alone BSP also includes SW demos with 3 edge detection and 2 motion detection video processing designs. The edge detection demos support use of user defined ARM C code which is executing in parallel with the generated HW video processing paths. The motion detection demos support the pipelines of HW accelerators.

This application note [7] and the BSP package can be downloaded for free from the UTIA public www server [8].

Main objectives of this application note are:

- To demonstrate how to install, compile, modify and use the BSP and SW projects in the Xilinx SDSoC 2015.4 [5] for the Trenz TE0701-05 platform with Zynq XC7Z020-2CLG484I device and HDMII-HDMIO support.
- To demonstrate the HW accelerated video processing algorithms and the speedup against SW versions.

Figure 1: TE0701-05 platform, Zynq XC7Z020-2CLG484I device and HDMII-HDMIO support.

Figure 2: HW accelerated edge detection in Full HD, 60 FPS, with 3 HW accelerators (sh03 demo).

The demo sh03 running in *Figure 2* is executing edge detection with 3 HW data paths. The size (number of micro-lines) processed by the edge detection filters is can be set in the runtime. Demo is controlled from the SDSoC user-defined C/C++ code running on ARM. The ARM processor can also perform user-defined, synchronous computation in parallel to the HW data paths.

Common setup for all included demos:

- ARM Cortex A9 processor of Xilinx Zynq device XC7Z020-2I executes standalone C application programs performing initialisation and synchronisation of the HW accelerated video processing chains.
- Enclosed C programs can be modified by the user and recompiled in Xilinx SDSOC 2015.4.
- Compiled demos can boot from the SD card directly after the power ON.
- Video data are provided by a Full HD HDMI source with resolution 1920x1080p60 (laptop).
- Data are processed in HW into the YCrCb 16 bit per pixel format and stored by video DMA (VDMA) controller to input video frame buffers (VFBs) reserved in the DDR3. This is done by the BSP HW.
- In case of SDSoC compilation (with selected HW accelerated C/C++ functions) the generated HW DMA controllers send data from the input VFBs to the processing HW accelerators in the programmable logic (PL) part of Zynq and another HW DMA controllers send processed data from HW to output VFBs.
- Second part of the HW VDMA IP core is sending data to the Full HD display (1920x1080p60). This is done by the BSP HW and it is identical for the SDSoC SW and HW compilation target.

1.2 Introduction to the demos

Edge detection

The edge detection algorithm is producing B/W Full HD video stream. Edges in each frame are marked as white and remaining part of the figure is set as black.

The edges are detected by a Sobel filter. Each pixel is filtered by a 3x3 2D FIR filter. A nonlinear decision on the output of the filter provides information, if the pixel is part of an edge or not. All computation is performed in fixed point.

Demos **sh01**, **sh02** and **sh03** provide accelerated HW computation of edge detection with 1, 2 or 3 parallel HW data paths. HW demos are using 1, 2 or 3 DMA HW channels from the DDR3 to 1, 2 or 3 as an input to Sobel filters. Another 1, 2 or 3 DMA HW channels support output from the Sobel filters to the DDR3. Zynq PL resources and the accelerations reached for these HW designs are summarised in sections 1.3, 1.4 and 1.5.

Motion detection

The motion detection algorithm detects and performs visualisation of **moving edges**. The moving edges are identified by two Sobel filters performing FIR filtering (similar to the above described edge detection) on pixels with identical coordinates, but from two subsequent video frames. The difference of these two filtered signals is filtered by a Median filter. The resulting signal is used for the nonlinear binary decision about the pixel. If the pixel is part of a moving edge, it is assigned red colour and merged with the original colour video signal. Resulting output Full HD video signal is unchanged, with the exception of red colour marked moving edges. See *Figure 2*. The fast moving edges in the face of the rabbit are marked by red pixels.

Demos **md01** and **md02** provide accelerated HW computation with 1 or 2 parallel HW data paths. HW demos are using 2 or 4 DMA HW channels for reading from **two** subsequent video frame buffers (located in the DDR3) to 1 or 2 video processing chains of HW accelerators performing the motion detection.
Another 1 or 2 DMA HW channels perform parallel write of results to the DDR3. Zynq PL resources and accelerations reached for these HW designs are summarised in sections 1.6 and 1.7.

Measurements of acceleration

The acceleration results have been measured as a ratio of the frame per second (FPS) reached by the HW accelerators generated by the SDSoC 2015.4 and the FPS reached by the SDSoC 2015.4 SW implementation on ARM compiled in the “SDRelease“ mode with the maximal SW optimisation (but without NEON) for the 32 bit ARM Cortex A9

1.3 Project sh01: Edge detection with single HW accelerator

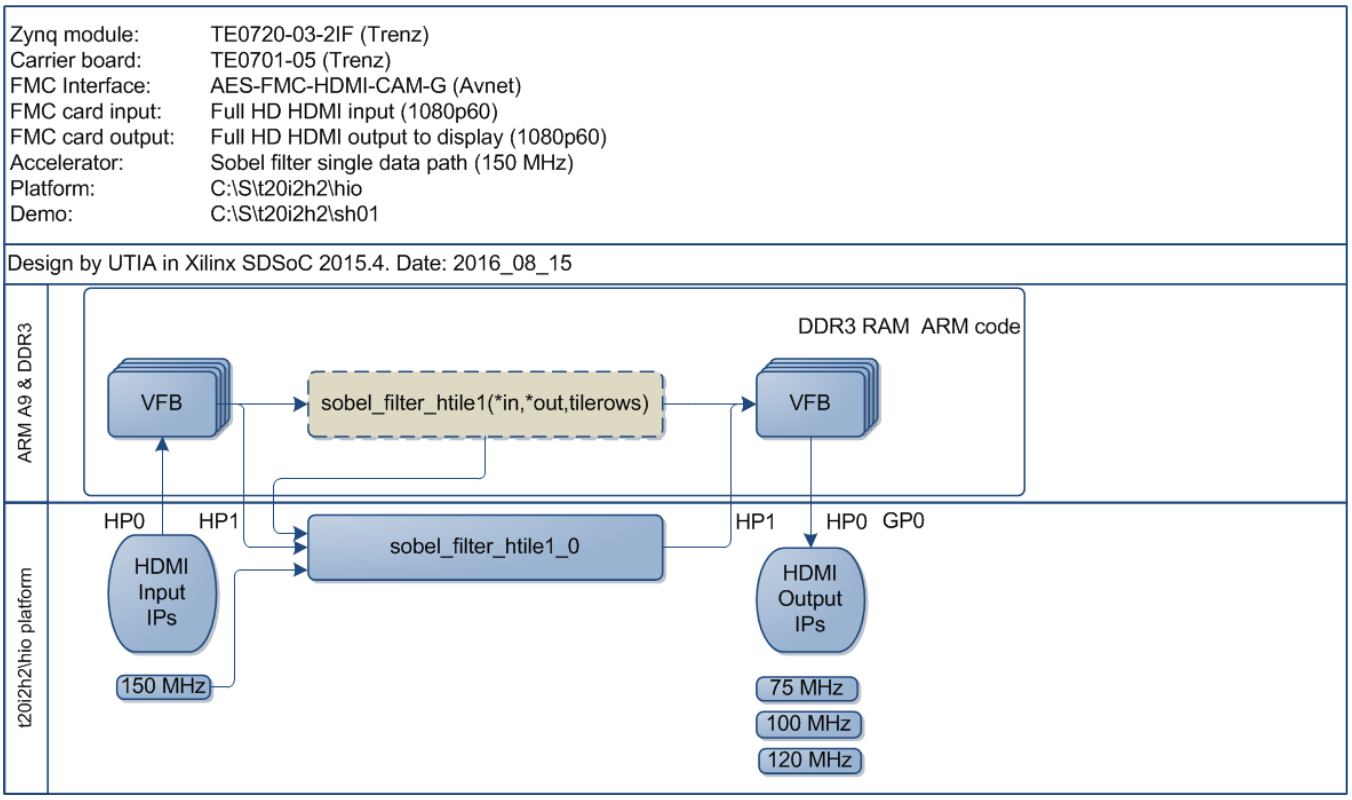
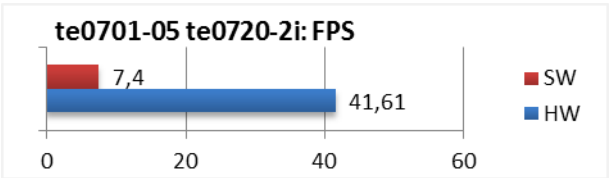
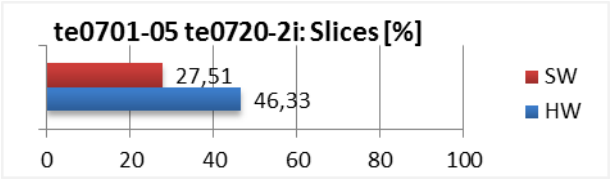


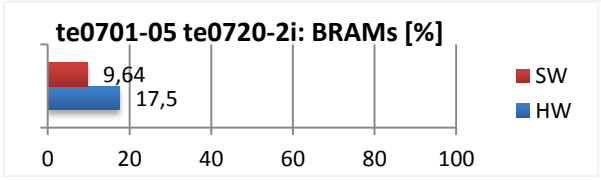
Figure 3: Project sh01 - Edge detection with single HW accelerator.

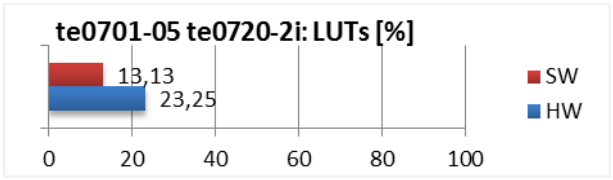
TE0720-03-2IF Sobel 1x

Acceleration by HW: 5.59 x









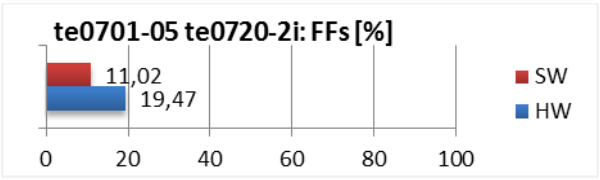


Figure 4: Project sh01 - Acceleration and HW resources used.

1.4 Project sh02: Edge detection with two HW accelerators

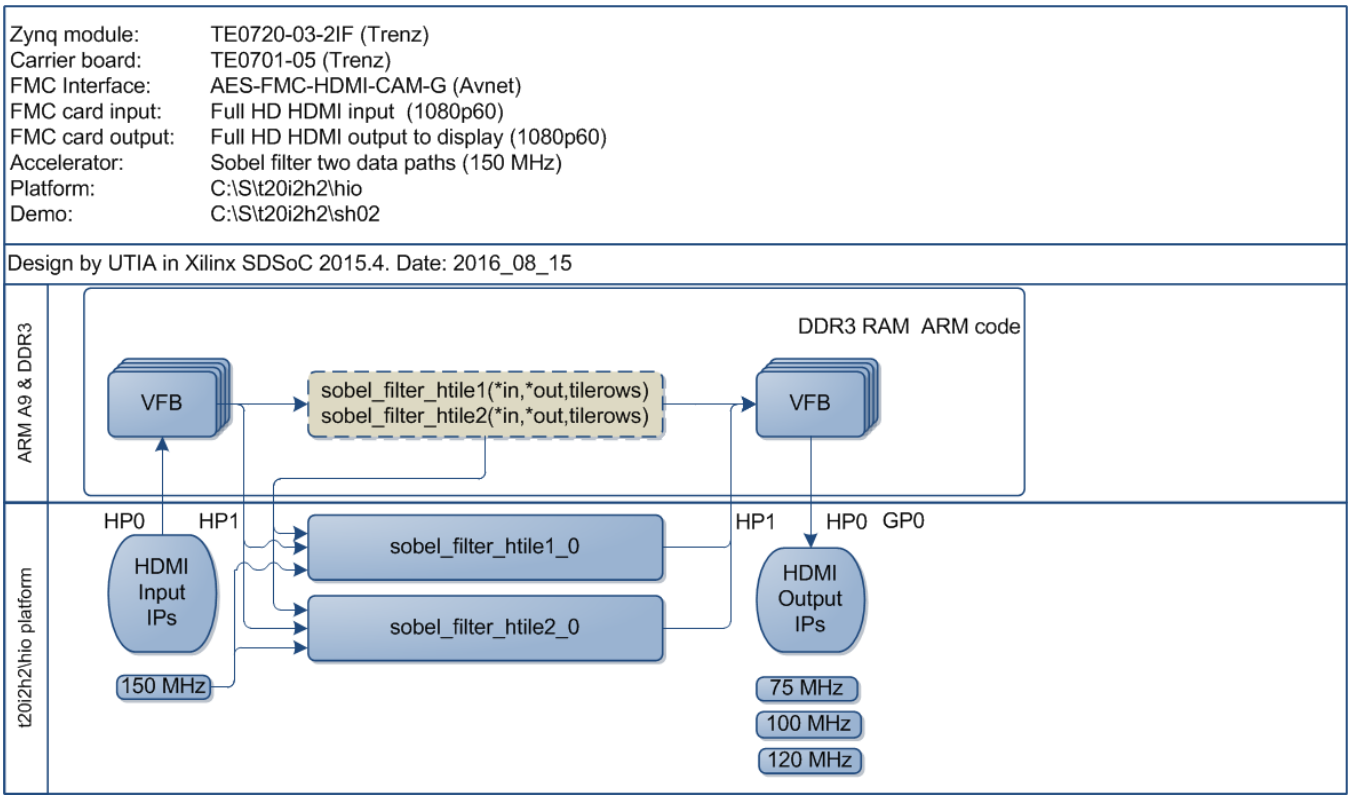


Figure 5: Project sh02 - Edge detection with two HW accelerators.

Figure 6: Project sh02 – Acceleration and HW resources used.

1.5 Project sh03: Edge detection with three HW accelerators

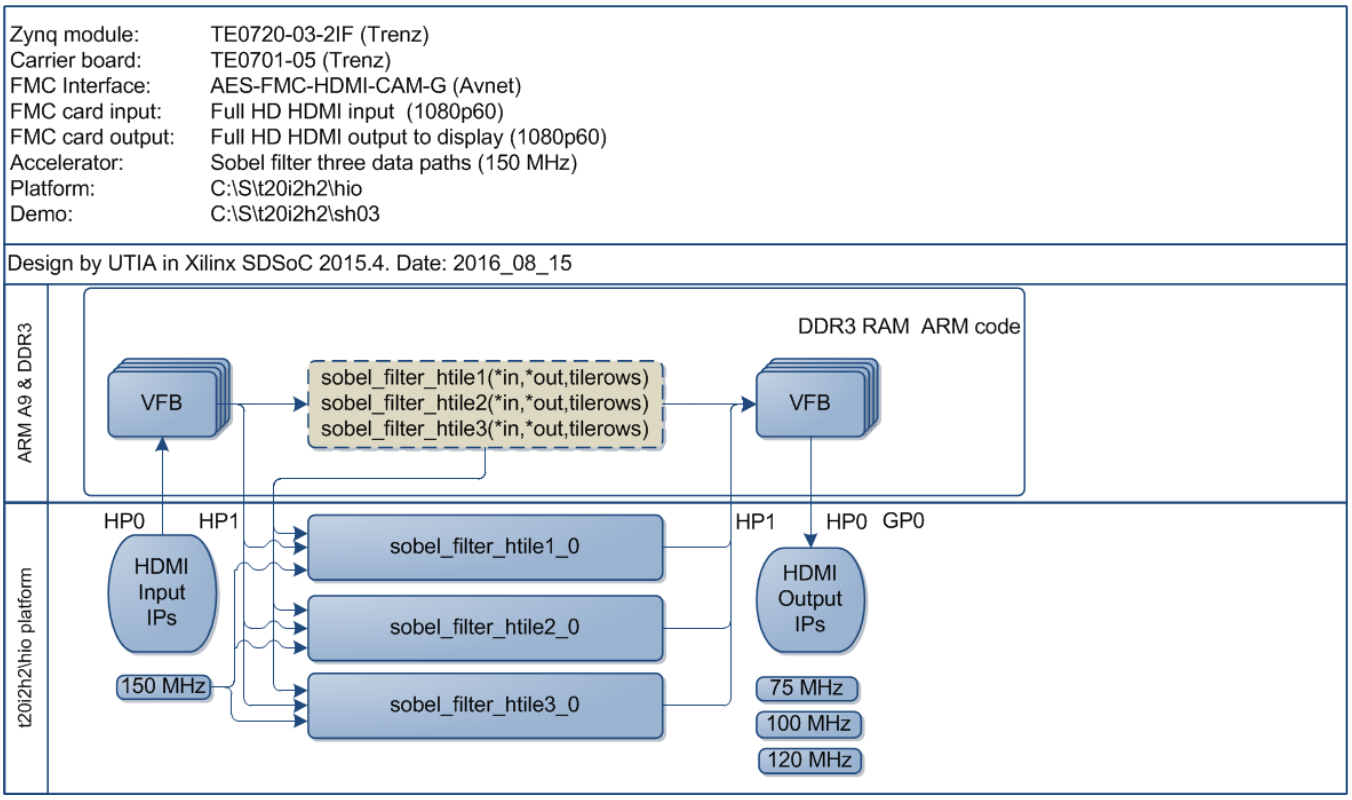
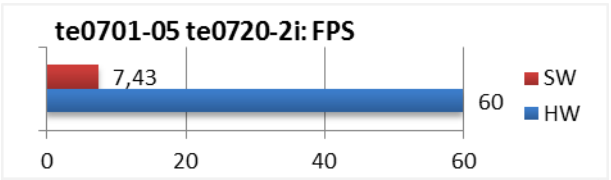
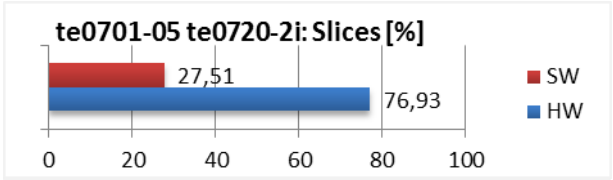


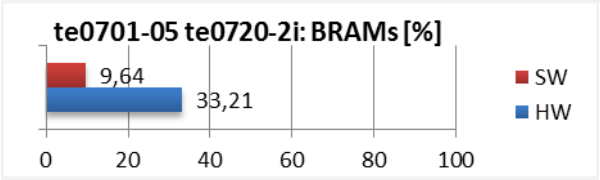
Figure 7: Project sh03 - Edge detection with three HW accelerators.

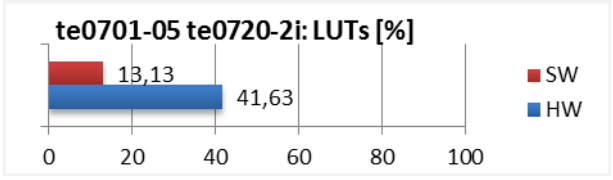
TE0720-03-2IF Sobel 3x

Acceleration by HW: 8.08 x









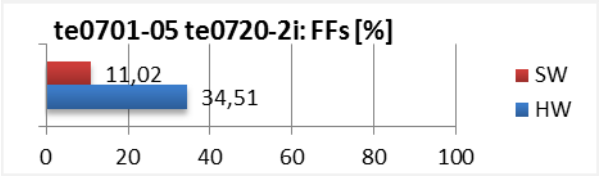


Figure 8: Project sh03 - Acceleration and HW resources used.

1.6 Project md01: Motion detection with single chain of HW accelerators

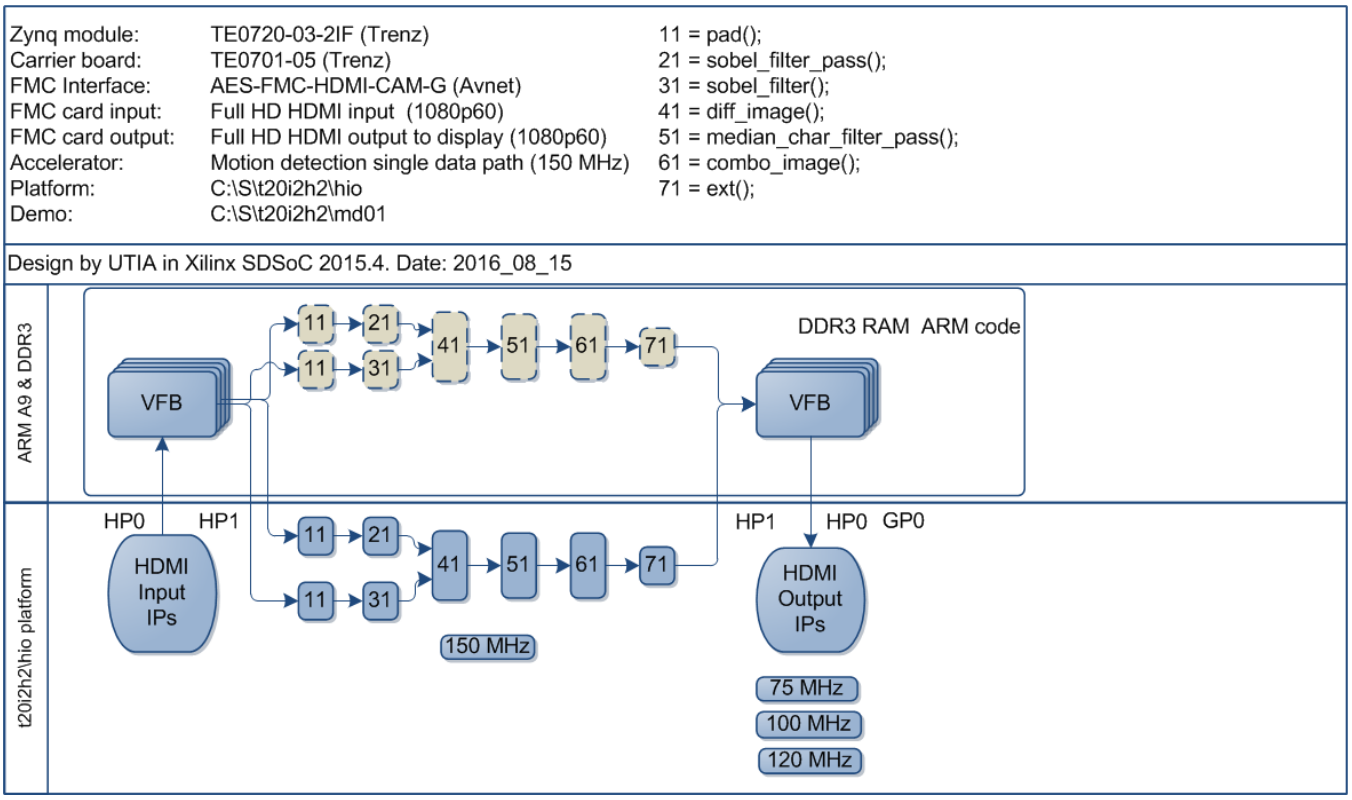
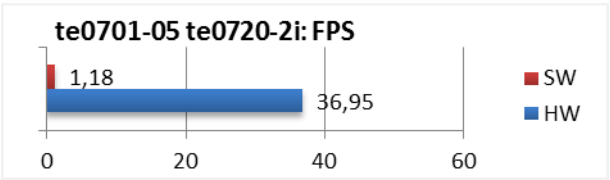
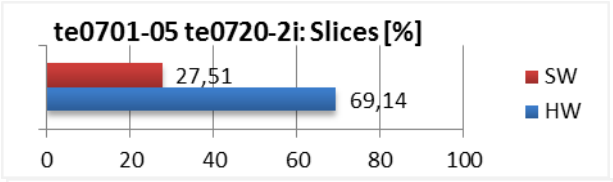


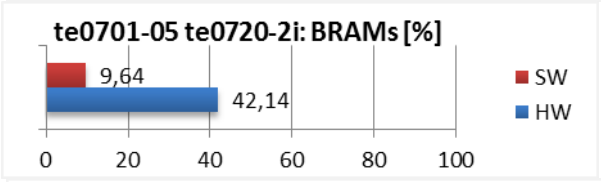
Figure 9: Project md01 - Motion detection with single HW accelerator data path.

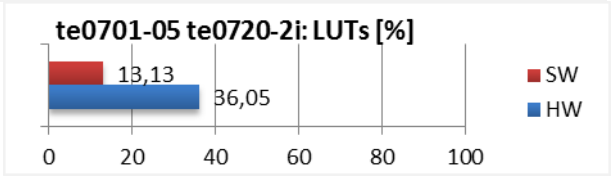
TE0720-03-2IF Motion Detection 1x

Acceleration by HW: 31.31 x









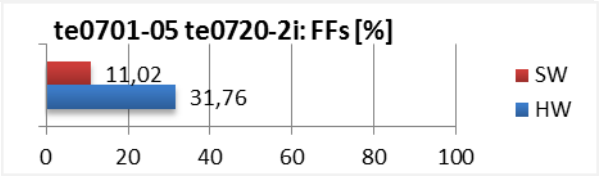


Figure 10: Project md01 - Acceleration and HW resources used

1.7 Project md02: Motion detection with two chains of HW accelerators

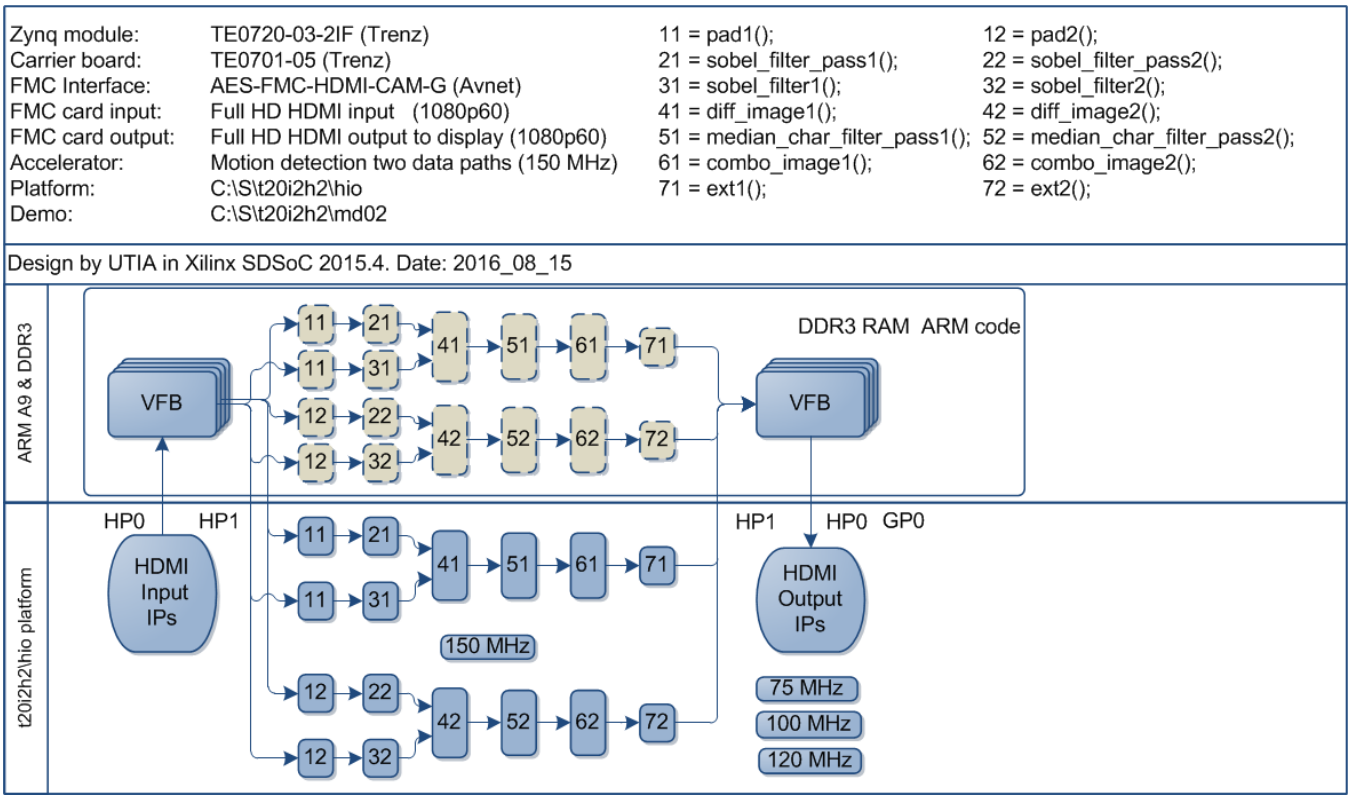


Figure 11: Project md02 - Motion detection with two HW accelerator data paths.

TE0720-03-2IF Motion Detection 2x

Acceleration by HW: 48.38 x

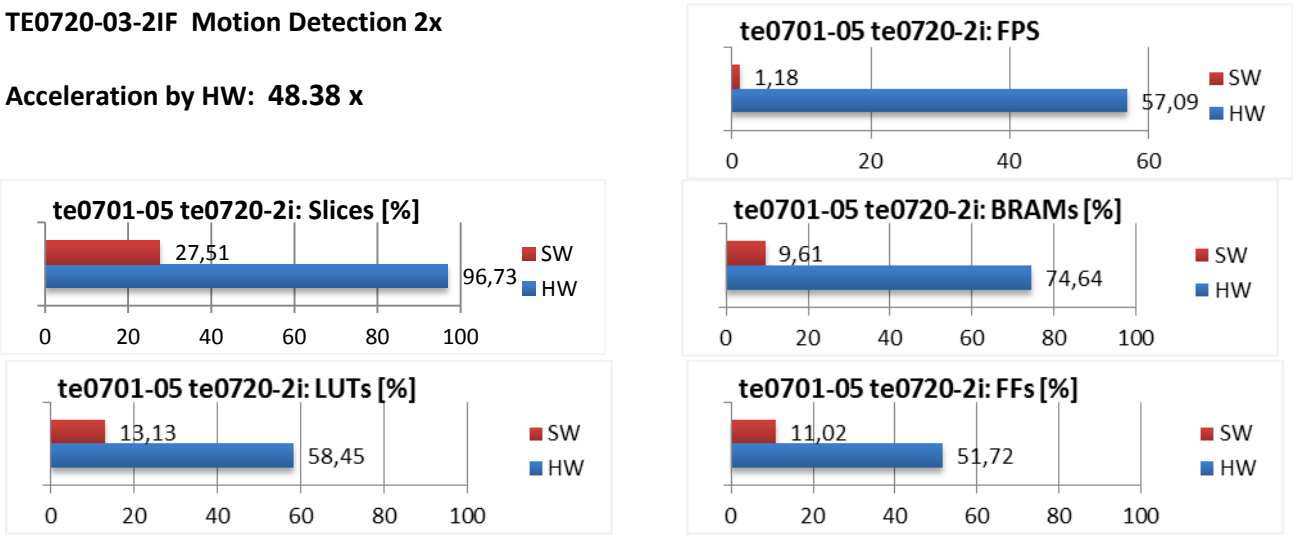


Figure 12: Project md02 - Acceleration and HW resources used.

2. Installation

2.1 Download the BSP for SDSoC 2015.4 and Demos

This application note can be downloaded as file [7]:
http://sp.utia.cz/results/t20i2h2/t20i2h2_2015_4.pdf
from UTIA public www server page [8]:
http://sp.utia.cz/index.php?ids=results&id=t20i2h2

The UTIA BSP package and demos can be downloaded from this page after registration. Fill your name and your e-mail). UTIA server will send to you the download link to the e-mail you have provided. It is link to your temporary copy of the package created for your download. You will download the zip file:
t20i2h2.zip

Unzip the **t20i2h2.zip** content to the directory **C:\S** to get this file structure on your PC:
C:\S\t20i2h2_S54_IMPORT
C:\S\t20i2h2
C:\S\t20i2h2_S54_boot_files

The first directory includes SDSoC 2015.4 demos to be imported into new SDSoC 2015.4 project.
The second directory includes the SDSoC 2015.4 board support package **"t20i2h2\hio"** for the Trenz TE0701-05 carrier [3] and industrial grade Zynq XC7Z020-2IF device on System on Module TE0720-03-2IF [1] and Full HD HDMII-HDMIO FMC card.
The third directory includes precompiled BOOT.BIN files for fast evaluation of SW and HW versions of included demos. The BOOT.BIN files can be recompiled in the Xilinx SDSoC 2015.4 from the included source code.

2.2 Installation of Avnet HDMI In and HDMI Out IP Cores

The board support package for the Trenz TE0701-05 carrier works with Full HD HDMI input and Full HD HDMI output implemented on the Avnet FMC AES-FMC-HDMI-CAM-G board. Avnet provides documentation for the AES-FMC-HDMI-CAM-G board in the www page [4]:
http://products.avnet.com/shop/en/ema/3074457345623664802

The Avnet IP cores for Vivado 2015.4 **avnet_hdmi_in** and **avnet_hdmi_out** have to be downloaded.
Please, follow these steps:

1. Registration: If you are new you have to register on the Avnet server to be able to download files. Click on the green button: [SIGN IN/REGISTER]
2. After sign-in or registration, you can immediately download the file:
   AES-FMC-HDMI-CAM-G-FMCHC_PYTHON1300C_Tutorial_2015_4_01.zip
   from the Avnet AES-FMC-HDMI-CAM-G board www page [4].
3. Unzip the downloaded file and open the included pdf tutorial:
   FMCHC_PYTHON1300C_Tutorial_2015_4_01.pdf
4. Download the needed zip file with Avnet design files and IP cores (as described in section Experiment 2 on page 4-5) of the Avnet tutorial:
   hdl-fmchc_python1300c_PZ7030_FMC2_20160223_221823.zip
5. This zip file includes the needed Vivado 2015.4 IP cores for Avnet the AES-FMC-HDMI-CAM-G:
   \IP\avnet_hdmi_in
   \IP\avnet_hdmi_out
   \IP\interfaces

The BSP package **t20i2h2.zip** downloaded from UTIA server contains an empty directory:

C:\S\t20i2h2\hio\vivado\hio.ipdefs\ip-imageon_0

Copy the downloaded Avnet IP cores to this empty directory to get following file structure of the BSP:

C:\S\t20i2h2\hio\vivado\hio.ipdefs\ip-imageon_0\avnet_hdmi_in
C:\S\t20i2h2\hio\vivado\hio.ipdefs\ip-imageon_0\avnet_hdmi_out
C:\S\t20i2h2\hio\vivado\hio.ipdefs\ip-imageon_0\interfaces

The standalone **"t20i2h2\hio"** BSP for the Trenz TE0701-05 carrier [3] with industrial grade Zynq XC7Z020-2IF device on System on Module TE0720-03-2IF [1] with the Full HD HDMII-HDMIO support is complete and ready for use. All needed IP cores are installed to the SDSoC 2015.4 now.

2.3 Download Trenz-Electronic Board Description Files for TE0720-03-2IF

The SDSoC 2015.4 board support package is Vivado 2015.4 project with some meta-data. It works with the Zynq xc7z020-2I part on the TE0720-03-2IF system on module. This Vivado 2015.4 project requires actual board description files for this module named TE0720-03-2IF. This set of files can be downloaded from the Trenz-Electronic server. Please, follow these steps.

1. Open www page:
   https://shop.trenz-electronic.de/de/TE0720-03-2IF-Xilinx-Zynq-module-XC7Z020-2CLG484I-ind.-temp.-range-1-Gbyte

2. Switch to the sub-page **Downloads** and follow this selection path:
   Reference Designs -> **2015.4** -> **test_board**. Download the needed file:

   TE0720-test_board_noprebuilt-vivado_2015.4-build_34_20160531091130.zip
   (Size 4,26 MB / Modified 31.05.2016 - 09:11:32)

3. This file contains the needed Vivado 2015.4 board description files **TE0720-2IF**

   test_board\board_files\TE0720-2IF

Copy these directories with all files to the installation directory of the SDSoC 2015.4.
You have to get this file structure:

C:\Xilinx\SDSoC\2015.4\Vivado\2015.4\data\boards\board_files\TE0720-2IF

This path is valid for a default location of Xilinx SDSoC 2015.4 tools. If your SDSoC installation is different, use that different location.

SDSoC 2015.4 is calling its Vivado 2015.4 installation. The expected board description files will be found in TE0720-2IF. The board description files for the TE0720-03-2IF module are ready for use, now.

The installation steps described in sections 2.1, 2.2 and 2.3 have to be done only once.

2.4 Import of the BSP and SW demos to new Xilinx SDSoC 2015.4 project

Start Xilinx SDsoC 2015.4 and select the directory for the SDSoC 2015.4 workspace. See Figure 15. Select **C:\S\ t20i2h2**

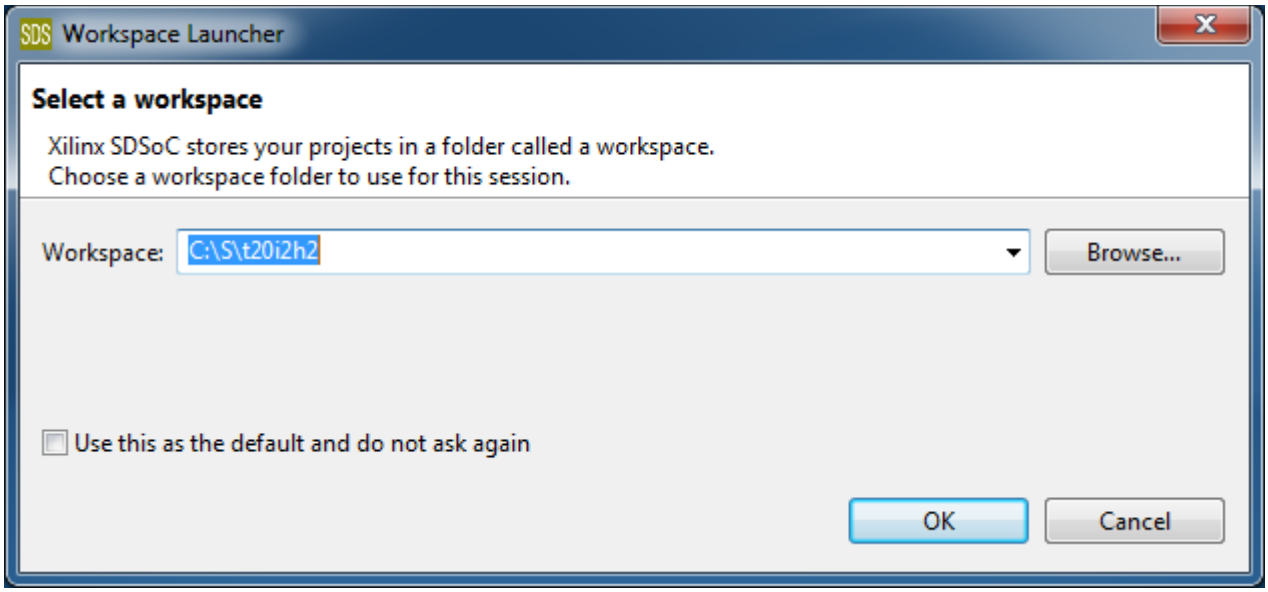


Figure 13: Select the SDSoC 2015.4 workspace.

HW and SW projects can be imported into SDK now. Select:
File -> Import -> General -> Existing Projects into Workspace
Click on Next button. See Figure 14.

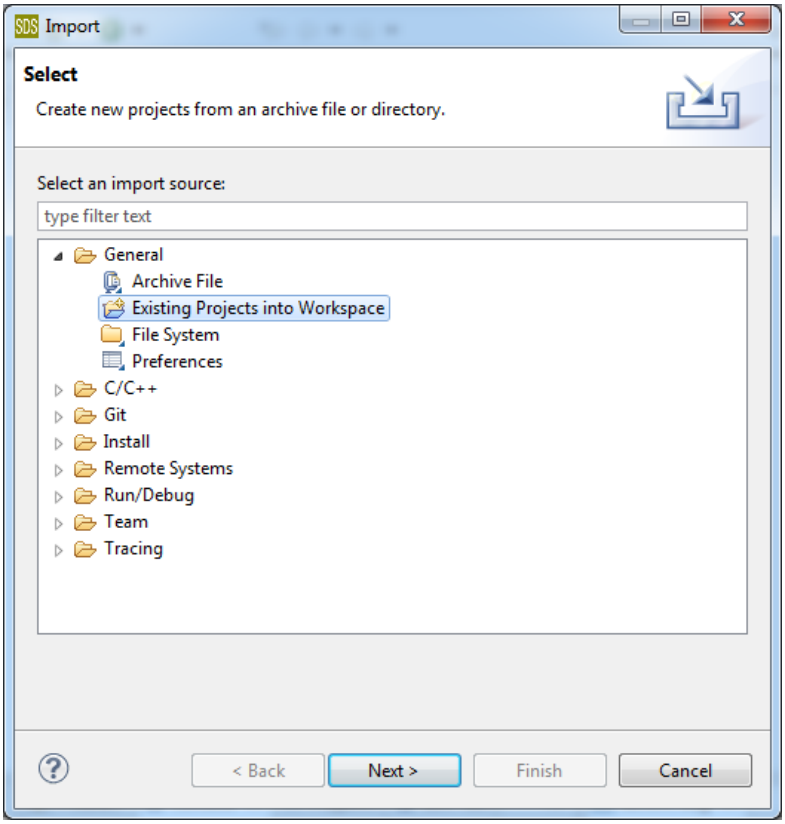


Figure 14: Import existing projects into workspace.

Type directory with projects to be imported. See Figure 15.

C:\S\t20i2h2_S54_IMPORT

Set the "**Copy projects into workspace**" check box.
Click on Finish button. See Figure 15.

Projects are imported. Compilation starts automatically.

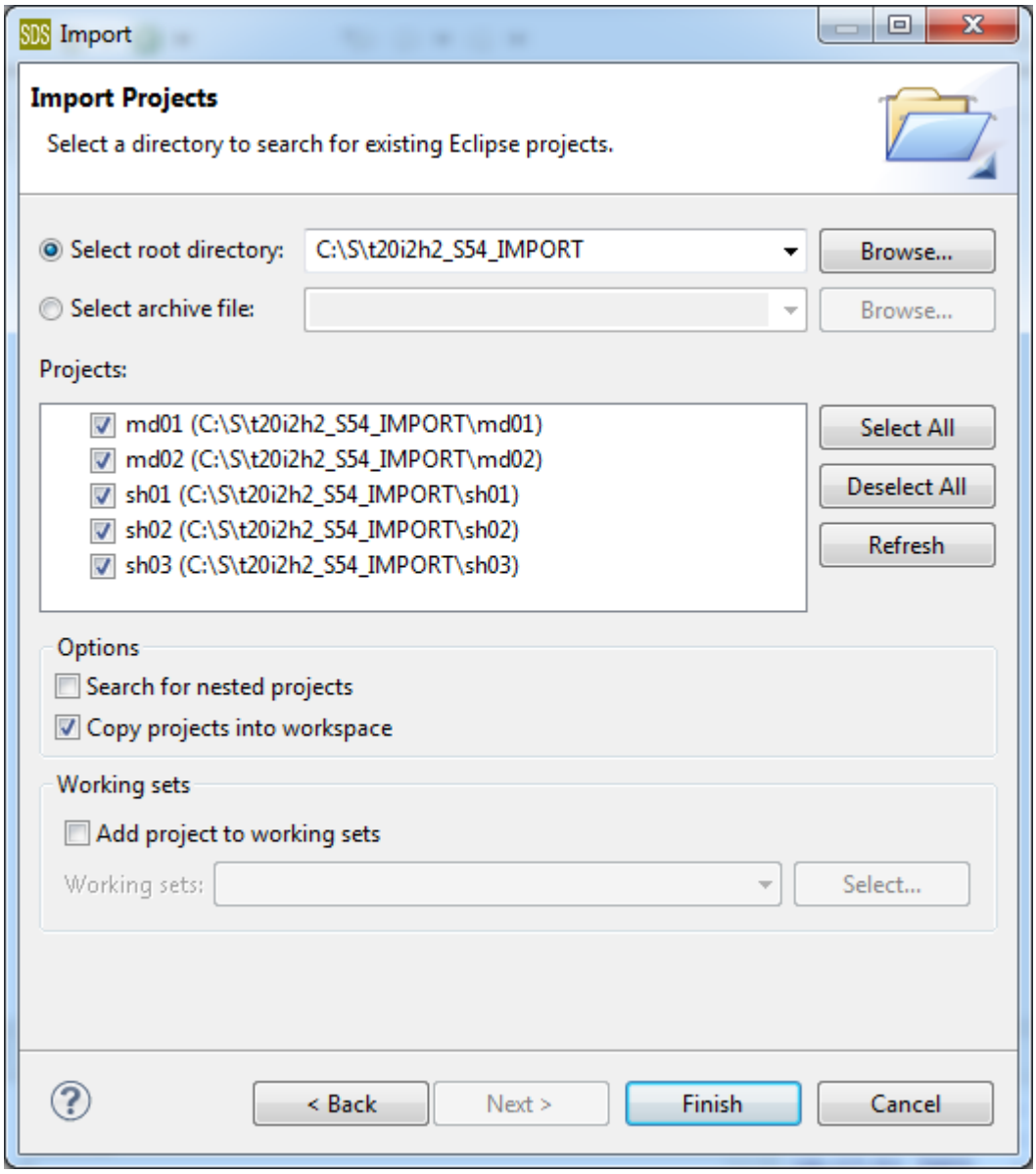


Figure 15: Select "Copy projects into workspace" and finish the import of all projects.

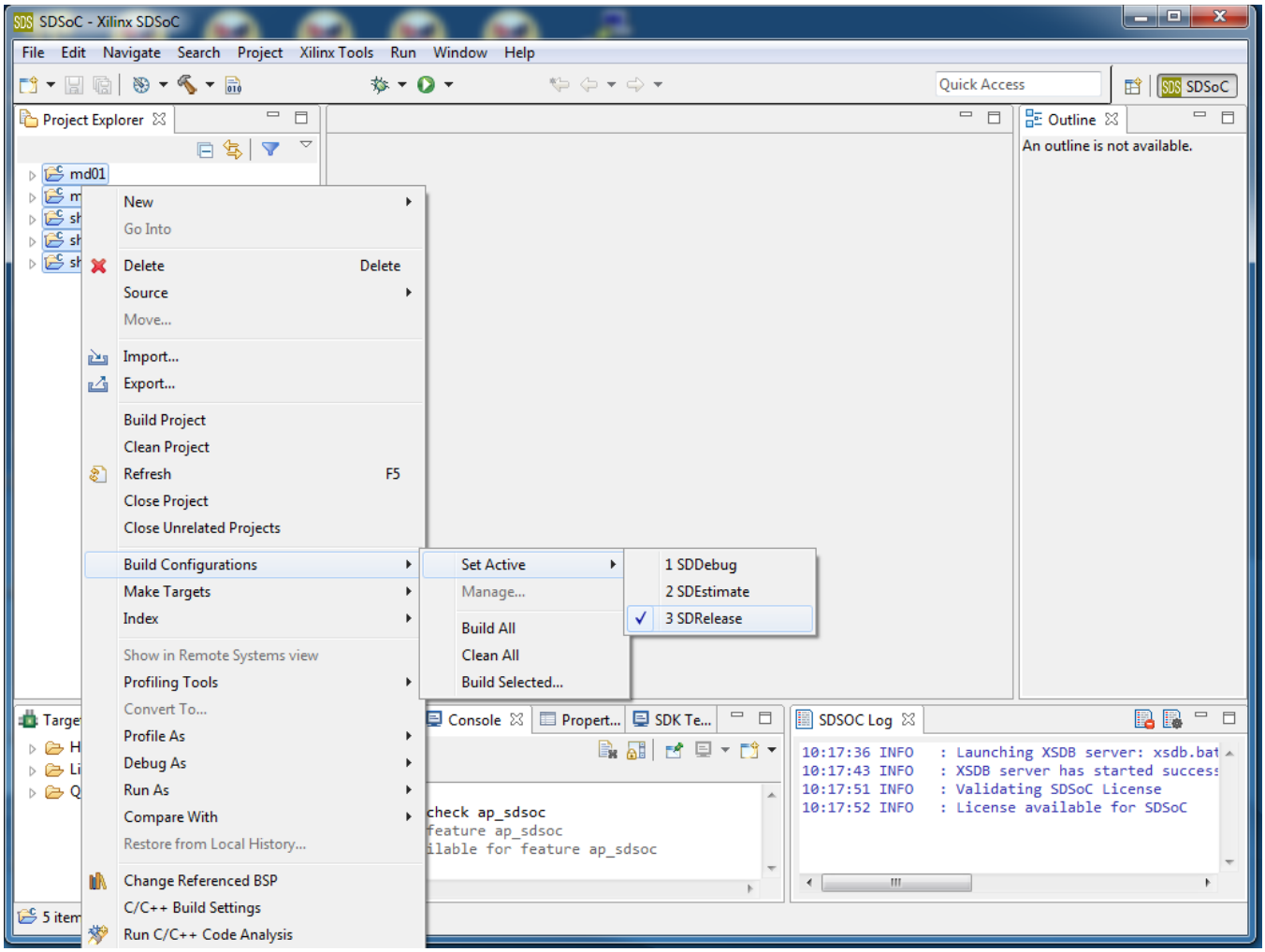


Figure 16: Select all projects to be compiled in SDRelease mode.

SDSoC 2015.4 environment compiles all imported demos in SDDebug mode by default. This default helps for debugging of ARM C code, but the real-time performance is lower.

Keep all projects highlighted and select the SDRelease mode for all imported projects to get maximal performance of SW demos.

Keep all projects highlighted and select “Build project”. This will compile the ARM SW version of all imported projects.

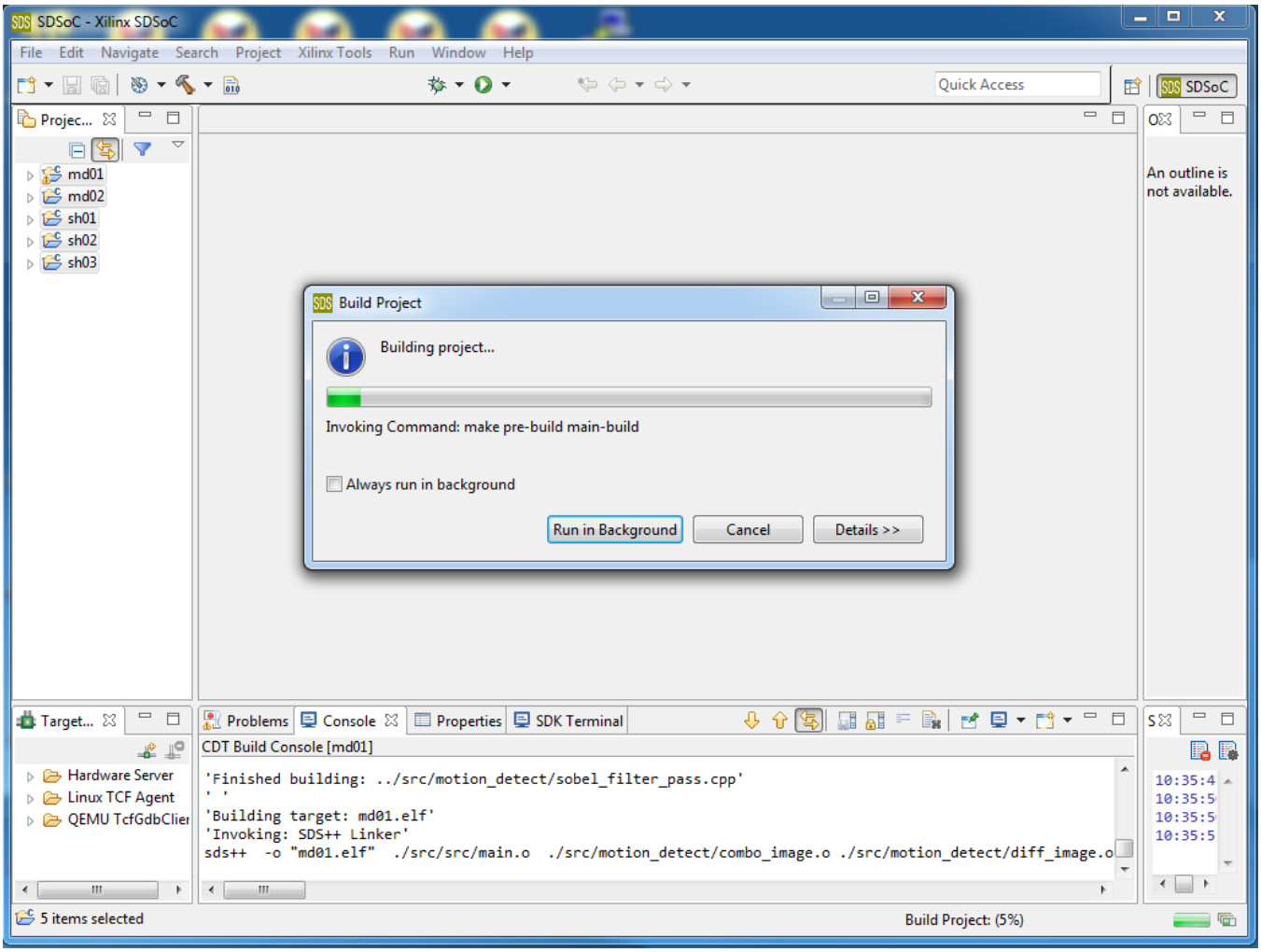


Figure 17: All projects are compiled in SDRelease mode.

SDSoC 2015.4 compiler compiles all imported demos. It takes approximately 1 minute for each project.

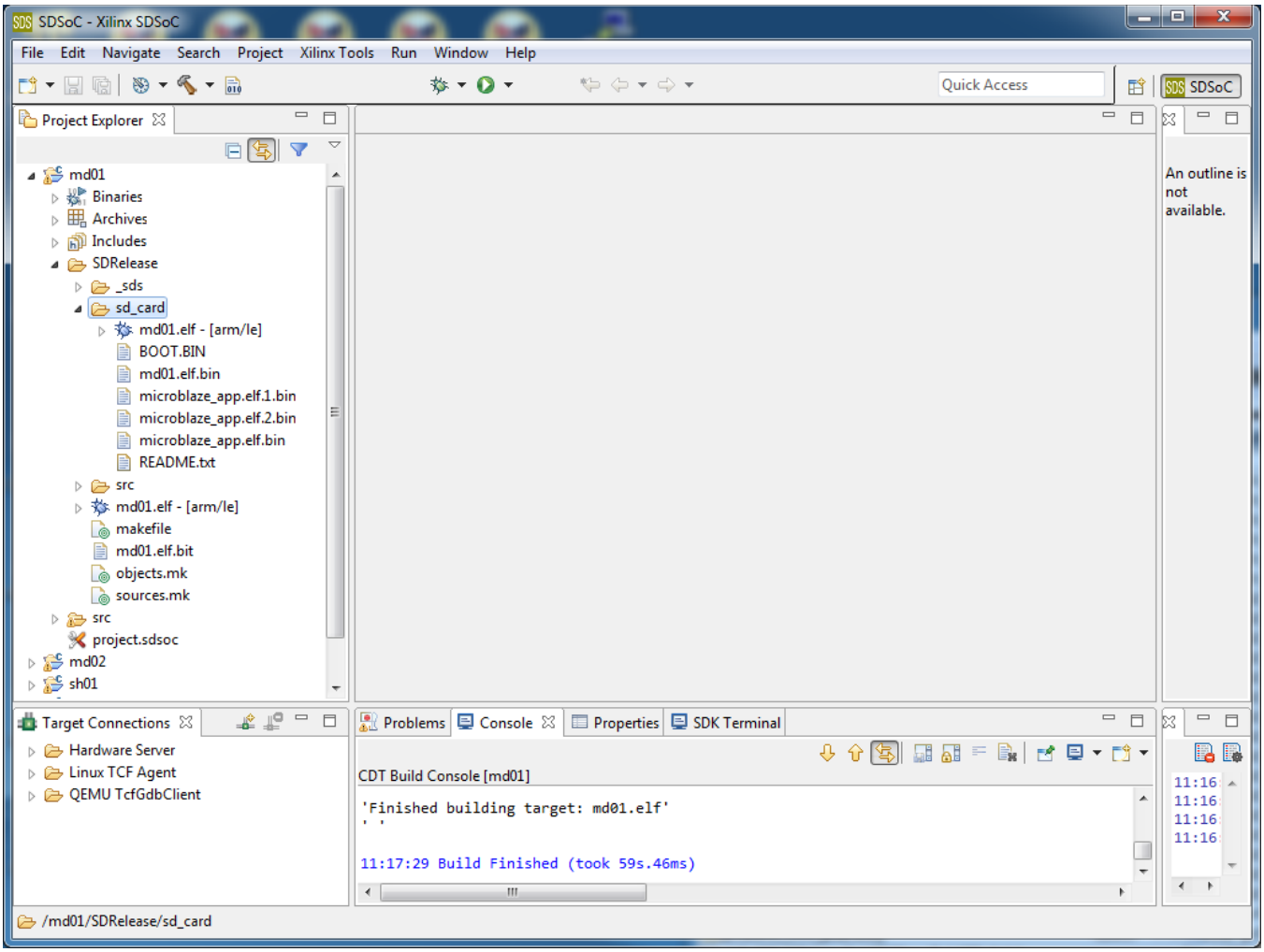


Figure 18: Each SW project creates BOOT.BIN file for the boot from the SD card.

SDSoC 2015.4 compiled all imported projects in SDRelease mode for standalone execution on ARM processor. Results of the compilation are the executable .elf files for ARM. These files are packed by the SDSoC 2015.4 together with the first stage boot loader executable and bitstream to the BOOT.BIN files created for each project. The generated BOOT.BIN files can be used for boot from the micro-SD card after the power-ON of the board. See Chapter 2.4 and Chapter 2.5 for explanations how to set up the HW board and how to test the compiled SW projects on the board.

2.5 Compilation to HW from SW source code in SDSOC 2015.4

- Select SW functions for HW acceleration as indicated in Table 1.
- Demo projects can be compiled separately or in a single batch in SDSoC 2015.4.
- Results of the compilation are again executable .elf files for ARM processor. Each .elf file is packed together with the first stage boot loader executable and the new generated bitstream to the updated BOOT.BIN file.

Time needed for compilation to HW (Intel i5 processor; 64bit; 3.4 GHz; RAM 32 GB):
sh01 **29 min**; sh02 **38 min**; sh03 **48 min**; md01 **52 min**; md02 **83 min**.

The generated BOOT.BIN files can be used to boot the system from the SD card after reset.

2.6 Compilation of HW accelerated projects

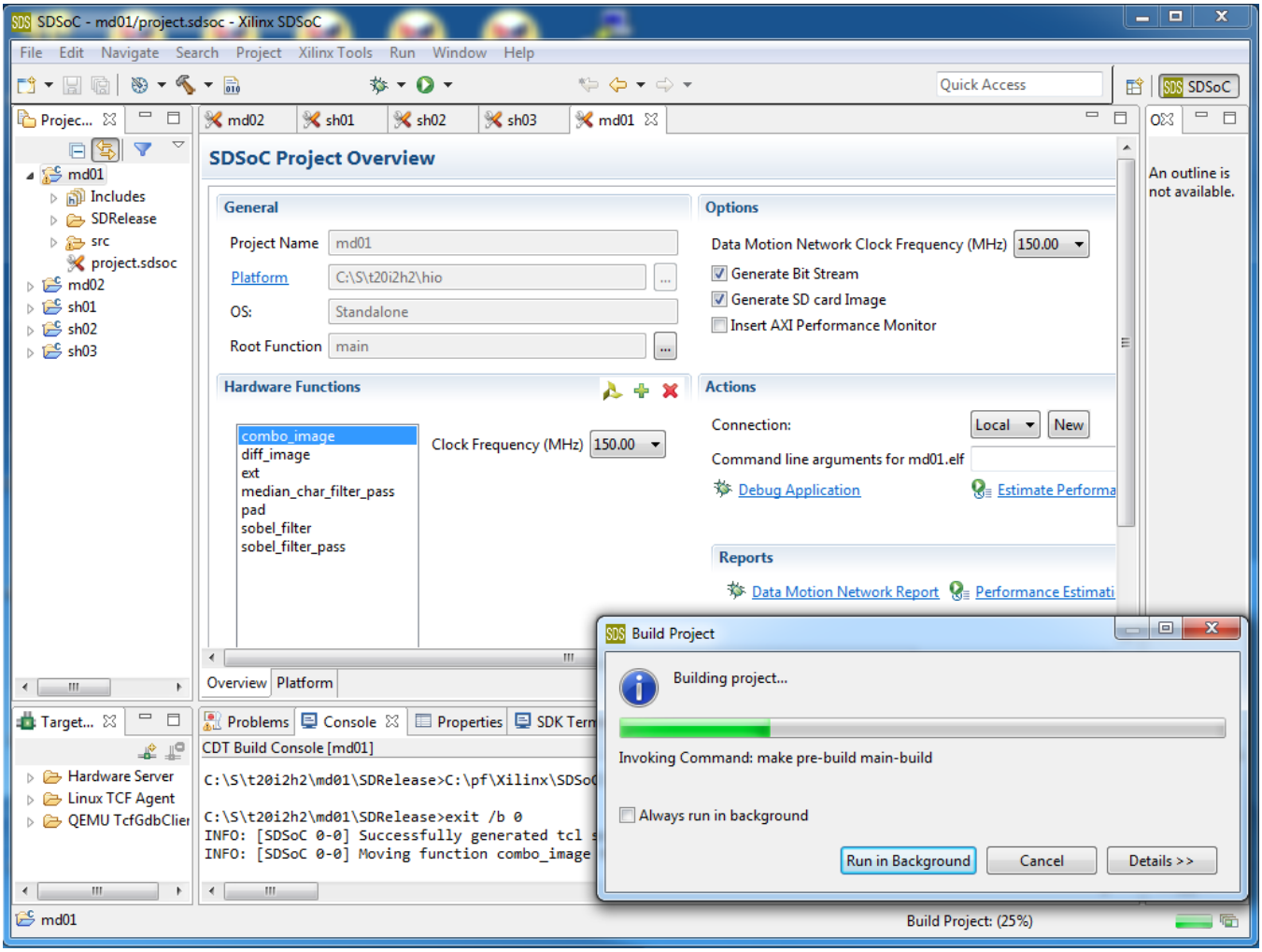


Figure 19: Selection of C/C++ functions for HW compilation in demo md01.

Select these C/C++ functions for SDSoC 2015.4 HW compilation.

Demo	Select C/C++ functions for HW acceleration
md01	combo_image diff_image ext median_char_filter_pass pad sobel_filter sobel_filter_pass
md02	combo_image1 diff_image1 ext1 median_char_filter_pass1 pad1 sobel_filter1 sobel_filter_pass1 combo_image2 diff_image2 ext2 median_char_filter_pass2 pad2 sobel_filter2 sobel_filter_pass2
sh01	sobel_filter_htile1
sh02	sobel_filter_htile1 sobel_filter_htile2
sh03	sobel_filter_htile1 sobel_filter_htile2 sobel_filter_htile3

Table 1: Selection of C/C++ functions for SDSoC HW compilation in all demos

Table 1 provides selection of SW function for the compilation by SDSoC 2015.4 environment.

2.7 HW setup

HW setup is using commercially accessible components [1], [2], [3], [4]:

TE0720-03-2IF; Part: XC7Z020-2CLG484I; 1 GByte DDR; Industrial Grade; [1]
Heatsink for TE0720, spring-loaded embedded; [2]
TE0701-05 Carrier Board for Trenz Electronic 7 Series; [3]
AES-FMC-HDMI-CAM-G FMC card with HDMI I/O and CAM interface [4]

HW Options:

TE0720-03-2IF	can be replaced by	**TE0720-02-2IF**	(Both boards are from Trenz) [1].
TE0701-05	can be replaced by	**TE0701-04**	(Both boards are from Trenz) [3].

Trenz TE0701-04 or TE0701-05 carriers require modifications to run the FMC carrier AES-FMC-HDMI-CAM-G with Zynq TE0720-03-2IF system on module. The modification is related to the swapped polarity of the differential clock signal for the FMC board. Evaluation HW systems with carriers TE0701-04 or TE0701-05 provided by UTIA have these modifications already done.

UTIA can implement these HW modifications for the original Trenz TE0701-04 and TE0701-05 carriers. This requires written e-mail request to kadlec@utia.cas.cz . Request will be first confirmed by UTIA. The interested party has to cover the cost of shipment of the carrier board to/from UTIA. Modification can be done in 5 working days and it is offered free of charge.

2.8 Test demos

To test demos follow these steps:

- Connect source of the Full HD HDMI signal (usually PC or laptop) to the HDMI IN connector on the AES-FMC-HDMI-CAM-G FMC card.
- Connect Full HD HDMI (or DVI) monitor by HDMI cable to the HDMI OUT on the AES-FMC-HDMI-CAM-G FMC card.
- Switch the monitor ON.
- Connect the carrier board by USB-to-miniUSB cable to PC to support JTAG serial link and the standard serial terminal on same USB cable.
- Connect power supply (DC 12V).
- Open and configure the standard serial terminal client (PuTTY or similar) on PC.
  (Speed: 115200 baud; Data bits: 8; Stop bits: 1; Parity: None; Flow control: None.)
- Reset the board. Board will start first stage boot loader from internal flash as set up by Trenz. It is writing messages to the serial terminal. On request, “Hit any key to stop autoboot” type any key to stop the auto-boot of Linux.
- On your PC, copy the BOOT.BIN to the top root directory of the SD card.
- Boot the board from the SD card. Initiate the boot by pressing reset on the TE0701-05 carrier.
- See the demo and the frame rate. The SD card can be removed and rewritten on your PC, while the demo is still running.

End of tests:

- Close the serial terminal client SW on the PC.
- Switch-off the power for the TE0701-05 carrier board.

3. References

[1] TE0720-03-2IF; Part: XC7Z020-2CLG484I; 1 GByte DDR; Grade: Industrial.
https://shop.trenz-electronic.de/de/TE0720-03-2IF-Xilinx-Zynq-module-XC7Z020-2CLG484I-ind.-temp.-range-1-Gbyte

[2] Heatsink for TE0720, spring-loaded embedded.
https://shop.trenz-electronic.de/en/26922-Heatsink-for-TE0720-spring-loaded-embedded?c=38

[3] TE0701-05 Carrier Board for Trenz Electronic 7 Series.
https://shop.trenz-electronic.de/en/TE0701-05-Carrier-Board-for-Trenz-Electronic-7-Series

[4] AES-FMC-HDMI-CAM-G; FMC card with Full HD HDMI I/O and CAM interface.
http://products.avnet.com/shop/en/ema/3074457345623664802

[5] Vivado HLx Web Install Client - 2015.4.
http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/2015-4.html

[6] SDSoC - 2015.4 Full Product Installation.
http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/sdx-development-environments/sdsoc/2015-4.html

[7] Jiri Kadlec, Zdenek Pohl, Lukas Kohut: SDSoC 2015.4 Standalone BSP with Full HD HDMI In-Out SW and HW Demos for Zynq System-on-Module TE0720-03-2IF and TE0701-05 Carrier Board. UTIA application note. Released 15.8.2016 on UTIA www server.
http://sp.utia.cz/results/t20i2h2/t20i2h2_2015_4.pdf

[8] UTIA public www server page for download of the application note [7], and the BSP package with demos for the Xilinx SDSoC 2015.4 environment.
http://sp.utia.cz/index.php?ids=results&id=t20i2h2

4. License

This stand-alone board support package (BSP) **"t20i2h2\hio"** for the Xilinx SDSoC 2015.4 [6] for the Trenz TE0701-05 platform [3] with industrial grade Zynq XC7Z020-2CLG484I device on System on Module TE0720-03-2IF [1] contains these deliverables:

- Board support package **"t20i2h2\hio"** for the Trenz TE0701-05 platform [3] with industrial grade Zynq XC7Z020-2CLG484I device on System on Module TE0720-03-2IF [1].
- 3 edge detection video processing demos (sh01, sh02 and sh03).
- 2 motion detection video processing demos (md01, md02).

The standalone BSP package **"t20i2h2\hio"** includes static library for ARM Cortex A9 processor (32bit) executing programs in the standalone mode:

libfmc_imageon.a.

- It is static library with interface functions for video IP cores.
- This library has no time restriction.
- Source code of this UTIA library is **not** part of the package.

The standalone BSP package **"t20i2h2\hio"** can be downloaded by a customer from the public UTIA www server [8] **free of charge** as zip file **t20i2h2.zip .**

UTIA is granting to the customer the time-unlimited, non-exclusive, non-transferable license for use of the stabdalone BSP package **"t20i2h2\hio"** on the customer site for SW and HW designs performed in the Xilinx SDSoC 2015.4 environment [6] and targeting the Trenz TE0701-05 platform [3] with industrial grade Zynq XC7Z020-2CLG484I device on System on Module TE0720-03-2IF [1].

The Xilinx SDSoC 2015.4 environment [6] is separate product from Xilinx. The SDSoC 2015.4 environment is not part of this package and it is not covered by this license. Licensing of the SDSoC 2015.4 [6] is provided separately by Xilinx.

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