RECONF

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Design methodology and environment for dynamically RECONFigurable FPGAs

Project Goals

- **Research dynamically re-configurable FPGAs** to allow implementation of adaptive system architectures by
  - Defining an adapted **design methodology**
  - Developing the required **design environment**

- **Demonstrate full benefits** of dynamically re-configurable FPGAs.

- **Validate methodology and tools** through industrial experiments

- **Demonstrate new opportunities** for large and small companies

- **Discuss technical advantages**
  - Easy applications upgrade,
  - Low power consumption,
  - Re-use

Results

- **Design methodology and design guidelines** with practical examples for Atmel AT40K/AT94K and Xilinx Spartan2/VirtexII **(UTIA, UPC, MBDA, Atmel, Kayser)**

- **New front-end tools (UPC)**
  - Dynamic Re-configuration Management Tool - System Level
  - Data Management Tool

- **New back-end tools (Atmel)**
  - Modular Place & Route Tool
  - FPGA Re-configuration Tool

- **Complete validation over four different and complementary issues with applications from different domains**
  - States Machine, Control   Space   **(Kayser)**
  - Complex algorithms & real time   Video   **(Deltatec)**
  - Data management, test & debug   Aeronautic   **(MBDA)**
  - Power & price issues   DSP Audio   **(UTIA)**

Examples