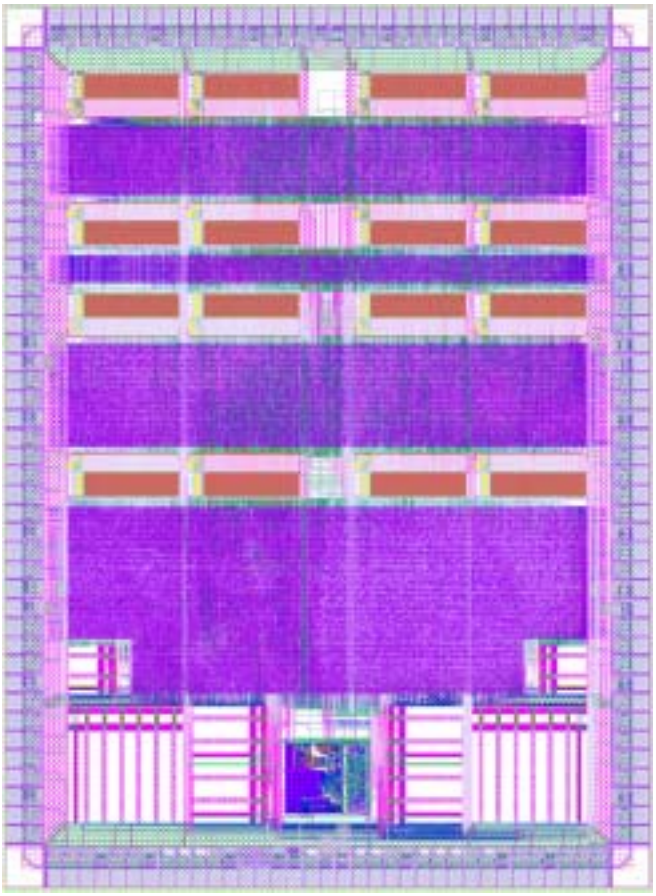
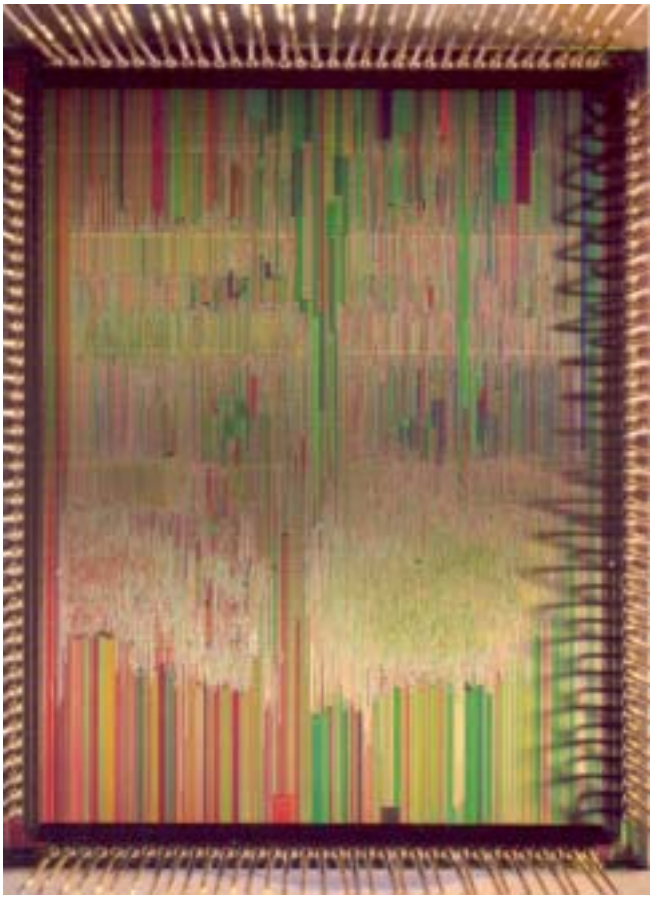
European Logarithmic Microprocessor

- SIMD logarithmic microprocessor with 32-bit data path
- Theoretical peak performance 650MFLOP equivalent at 166MHz
- SIMD instruction set (2-way real add/sub, 4-way for other operations)
- 4 stage pipeline with static branch prediction
- Upto 2 real add/subtract with 3/4 cycle latency
- Upto 4 real multiply/divide/square-root per cycle
- Internal Harvard architecture served by independent 2-way set-associative caches
- Register-memory operations for easy programming and high code density
- High bandwith 64-bit data-bus
- Built-in 2-channel DMA controller
- Technology CMOS 0.18μm, die size 13 mm^2
- Clock frequency 150MHz, power dissipation 150mW





Available as:	**Contact:**
25 samples packaged and ready for prototyping 25 samples ready for packaging *This work was funded by ESPRIT 33544 long-term research project with acronym HSLA.* **http://napier.ncl.ac.uk/elm**	Rudolf Matousek Department of Signal Processing Institute of Information Theory and Automation Prague, Czech Republic Tel: +420-2 6605 2264 Fax: +420-2 6605 2511 matousek@utia.cas.cz http://www.utia.cas.cz/zs